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Low temperature coefficient bandgap voltage reference generator

Vijayalakshmi Naganadhan
Iowa State University

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by

Vijayalakshmi Naganadhan

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Randall Geiger
Doug Jacobson

The student author, whose presentation of the scholarship herein was approved by the program of study committee, is solely responsible for the content of this thesis. The Graduate College will ensure this thesis is globally accessible and will not permit alterations after a degree is conferred.

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ABSTRACT

The maximum achievable performance of almost all mixed-signal and radio frequency systems is dependent on the accuracy of voltage references. The bandgap voltage of silicon at zero Kelvin, V_{GO} is a physical constant with unit Volts. It is independent of process, supply voltage and temperature variations.

This work proposes a strategy for extracting V_{GO} and expressing it at the output of a voltage reference circuit. The concept is implemented in UMC 65nm process and the simulation results indicate that the circuit design can achieve very low temperature coefficients (<1ppm/°C). The proposed concept is validated using measurements and the associated constraints are carefully investigated. The measured output voltage reference of the two tested units record a temperature coefficient of 3.4ppm/°C and 4.57ppm/°C across the industrial temperature range (-40°C to 85°C).

CHAPTER 1: INTRODUCTION

Voltage references form an integral part of analog, mixed-signal and radio frequency systems. The maximal achievable performance of a system is highly dependent on the accuracy of the voltage reference [1]. The increasing requirements for high performance and precision systems have posed a need for a highly-accurate voltage reference which should have a very low sensitivity to variations in process, supply voltage, and temperature. The most common applications of voltage references are in analog-to-digital converters (ADC), digital-to-analog converters (DAC), power management ICs etc. and the performance of the system depends on the accuracy and low temperature coefficient (TC) properties of the reference.

The bandgap voltage of silicon is well characterized over temperature and the bandgap voltage at zero Kelvin is found to have a temperature independent behavior [2] over a wide range of temperatures. It is also independent of supply voltage and process variations and is highly stable [3]. Hence, most of the voltage references are designed to express V_{GO} at the output and are called bandgap references. This research work mainly focuses on the performance of the voltage reference across the temperatures ranging from -40°C to 125°C.

1.1 Principle of Bandgap Reference

The basic principle of a voltage reference circuit involves a weighted summation of a voltage/current that is proportional-to-absolute-temperature (PTAT) and a voltage/current that is complementary-to-absolute-temperature (CTAT) and thereby the resultant voltage/current will have zero-temperature coefficient (ZTC).

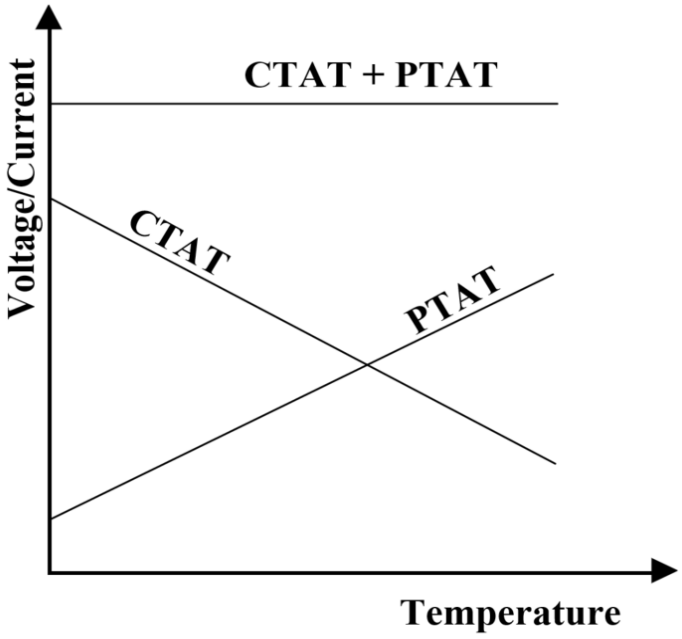


Figure 1: Behavior of an ideal bandgap reference circuit

There are various strategies and circuit structures used to implement the concept. Traditional bandgap reference circuits utilize the negative temperature dependence of the voltage across a PN-junction(diode) or base-emitter voltage, V_{BE} of a bipolar junction transistor (BJT) [3] while there are circuits that use gate-to-source voltage, V_{GS} of MOSFETs biased in the weak inversion or sub-threshold region, for this purpose [4], since they exhibit properties comparable to BJTs. While the former generates a highly accurate output voltage, the latter has lower power consumption [5]. The difference between the voltages across two PN-junctions or base-emitter voltages of bipolar junction transistors with varying current densities is used for the PTAT voltage generation. The thesis focuses on references that use diode-connected bipolar junction transistors for CTAT and PTAT voltage generation.

A simplified equation for generating the reference voltage is presented here [6], [7] while a detailed analysis explaining the temperature dependence of the associated parameters is presented in Appendix A. The I-V relationship for a bipolar junction transistor can be expressed as

$$I_C = I_S e^{\frac{V_{BE}}{NV_T}} \quad (1)$$

where V_{BE} is the base-emitter voltage of a diode or a diode-connected bipolar transistor, I_C is the collector current, I_S is the saturation current, N is the non-ideality factor (usually assumed to be 1) and V_T is the thermal voltage. (1) can be rearranged as

$$V_{BE} = NV_T \ln\left(\frac{I_C}{I_s}\right), \quad (2)$$

where ln(x) is the natural logarithm of x. I_S and V_T have temperature-dependent components that are responsible for the negative temperature dependence of V_{BE}.

$$I_S = CT^{\eta} e^{-\left(\frac{V_G(T)}{NV_T}\right)} \quad (3)$$

$$V_T = \frac{kT}{q} \quad (4)$$

where C is a temperature-independent constant (derivation in Appendix A) that includes emitter area A_e , η is a process-dependent constant, $V_G(T)$ is the bandgap voltage of Silicon, k is the Boltzmann's constant (8.62×10^{-5} eV/°K), T is the absolute temperature in Kelvin, q is the charge of an electron (1.602×10^{-19}C).

A circuit that generates the difference between the base-emitter voltages between two transistors operating at different current densities is used as a PTAT source. This can be implemented by making use of the difference in emitter areas of two bipolar junction transistors or difference in biasing currents or both.

If A_{e1} and A_{e2} are the emitter areas of the two bipolar junction transistors and I_1 and I_2 are the biasing currents, the difference between the base-emitter voltages of the BJTs is PTAT in nature and can be written as

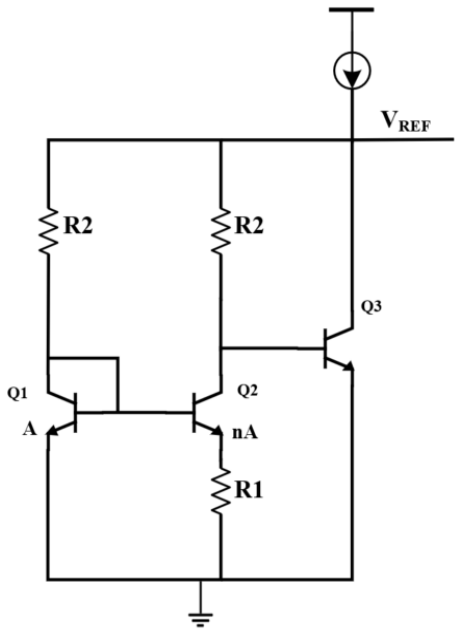
$$\Delta V_{BE} = V_{BE2} - V_{BE1} = NV_T \ln\left(\frac{A_{e1}}{A_{e2}} . \frac{I_2}{I_1}\right) \quad (5)$$

The output reference voltage can be expressed as (6), where the coefficients A_1 and A_2 are chosen to cancel the temperature dependencies of the respective terms. The expression of V_{BE} includes the extrapolated bandgap voltage at 0K, V_{GOr} (Appendix A) and the existing bandgap circuits are designed to express this quantity at the output.

$$V_{ref} = A_1 . V_{BE} + A_2 . \Delta V_{BE} \quad (6)$$

1.2 Various Architectures of Bandgap Reference Circuits

Even though the concept of using V_{GOr} as a standard for voltage reference was introduced by Hilbiber [3], a widely used version of the circuit was developed by Robert J. Widlar [8]. A few variants of the circuits were designed by Paul Brokaw [9], Karel E. Kuijk [10], H. Banba [11]. The implementation varies from one circuit to another, but the underlying concept remains the same. Figure 2 shows the widely used architectures of the bandgap reference circuits.



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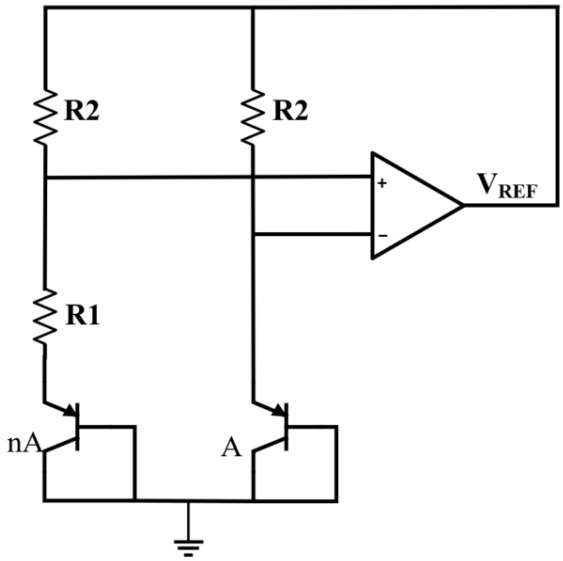
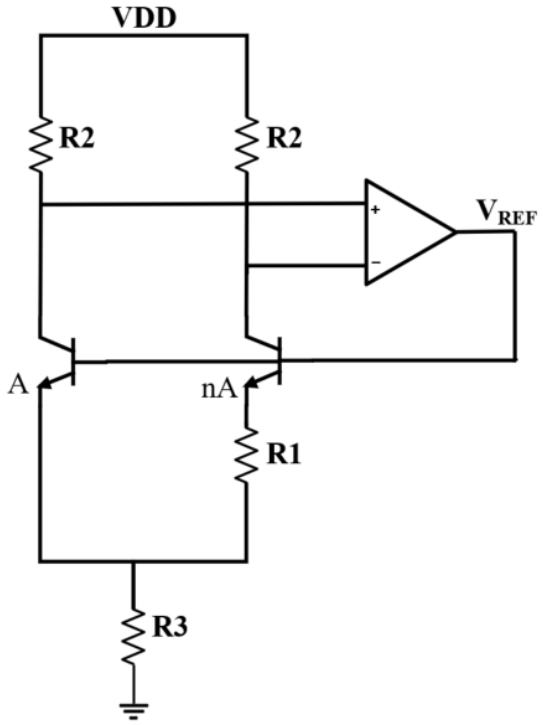


(2.2)

Figure 2 : Widely used Bandgap reference circuit architectures

(2.1) Widlar circuit [8], (2.2) Kuijk circuit [9] (2.3) Brokaw circuit [10], (2.4) Banba circuit [11]



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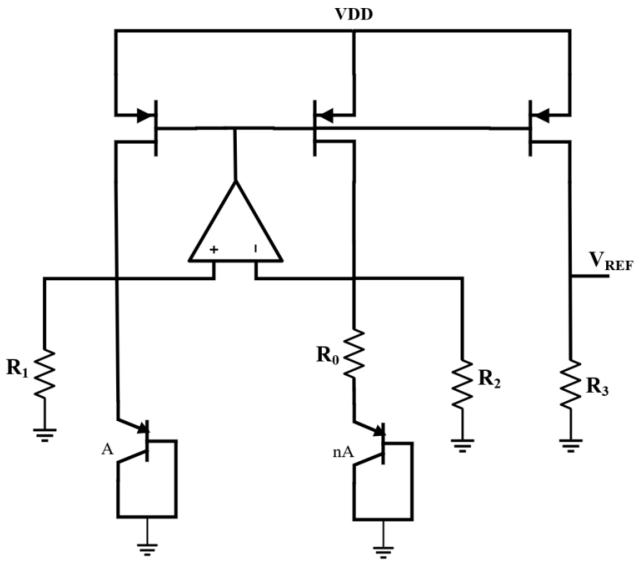


(2.4)

Figure 2 (continued)

1.3 Research Objective

Figure 3 shows a typical profile of the output reference voltage generated by the bandgap reference circuits shown above. It is evident that the output has a curvature as opposed to the expected constant voltage across temperature as shown in Figure 1.

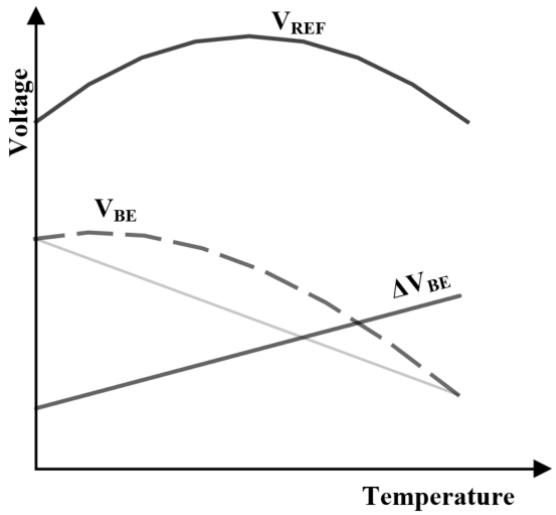


Figure 3 : Output voltage profile of first-order bandgap reference

The amount of variation in the reference voltage output with temperature is expressed in terms of the voltage temperature coefficient, TC (or drift specification in datasheet), which indicates the relative change in the voltage with a change in temperature. The definition of temperature coefficient used in this thesis is shown in (7). The most commonly used unit is parts per million/°C or ppm/°C.

$$\text{Temperature Coefficient(TC)} = \frac{V_{max} - V_{min}}{V_{max} * (T_{max} - T_{min})} * 10^6 \quad (7)$$

where V_{max} and V_{min} are the maximum and minimum output voltage values, and T_{max} and T_{min} represent the extremities of the temperature range over which the analysis is performed. The presence of the curvature in Figure 3 increases the TC of the reference.

Using Taylor series expansion $V_{BE}(T)$ can be expressed as a combination of a constant term, a linear term and a higher order non-linearity which is the main cause of the curvature in the output voltage reference. The circuits from [9]-[11] focus on the cancellation of the linear term and are called first order references. Hence, the output of such circuits would include V_{GOr} at the inflection temperature, Tr along with the remaining non-linearity in V_{BE}. But, a highly accurate reference would require the cancellation of this non-linearity and thereby compensates for the curvature.

Apart from the existing non-linearity of V_{BE}, there are a few non-ideal effects that are ignored in the equations but contribute to the temperature dependent performance of the circuit. As mentioned before, the bandgap references make use of two diodes or diode-connected bipolar transistors. Low cost CMOS processes have parasitic bipolar junction transistors, which can be configured as diodes. The associated properties like base resistance, current gain, β etc. can affect the performance of the bandgap reference circuits. A few effects of the non-linearities on the performance of the reference circuit have been analyzed in [12]. Due to the limited use of these devices, the complexity and the associated costs, the temperature dependent effects associated with these devices are not significantly investigated nor modeled in most of the available CMOS processes that use the Simplified Gummel Poon model for modeling the bipolar junction transistors. This makes it harder to design accurate bandgap references due to factors that have yet to be considered. A few advanced models like MEXTRAM and VBIC have better models for the parasitic transistors.

Stress during packaging can cause a shift in the temperature-dependent performance of bandgap reference circuits. A few studies [6], [13] have shown that the post-package

stress, which occurs due to the difference in the thermal expansion coefficients of the mold compound and the silicon die can cause a shift in the voltage relationship with temperature.

In this thesis, a curvature compensation scheme has been studied and implemented to design a reference circuit that can extract V_{GO} and achieve a sub-ppm/°C temperature coefficient. The various approaches take their shortcomings have been discussed before zeroing in on the adopted method. The design and simulation results of the V_{GO} extraction circuit are presented. A measurement set up used to validate the concept is detailed and the associated outcomes and observations are discussed.

This thesis is organized as follows. Chapter 2 describes the working of a basic first-order bandgap reference circuit and discusses the cause of the curvature in the output voltage. A few non-ideal effects that affect the performance of the circuit are analyzed in Chapter 3. Chapter 4 delves into the concept of curvature compensation and explains a few state-of-the art curvature compensation schemes. In Chapter 5, the adopted method of V_{GO} extraction is presented and a detailed design procedure is elucidated. The simulation results and the outcomes of each approach are explained in detail. Then, the chapter deals with the implementation of the proposed scheme and the various challenges that pose as a restriction. Chapter 6 describes the details of the measurement set-up used to validate the concept. The measurement results and observations are discussed. Finally, the conclusion and future works are detailed in Chapter 7. The detailed analytical derivation associated with the temperature dependency of V_{BE} and extraction of V_{GO} using temperature-dependent voltages, is presented in the Appendix.

CHAPTER 2: BANBA STRUCTURE FOR REFERENCE CURRENT GENERATION

The bandgap reference structure put forth by H. Banba [11] is commonly used in analog design circuits. The following section of the thesis focuses on this architecture.

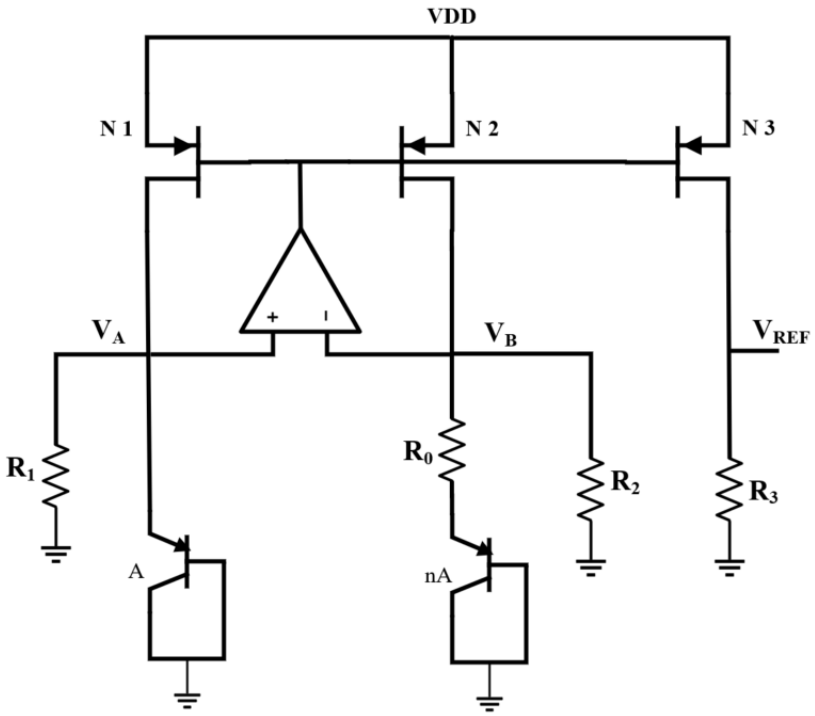


Figure 4: Banba bandgap reference circuit

2.1 Working of Banba Circuit

The key components of the circuits are the two key didoes Q1 and Q2 as explained in Chapter 1. Banba circuit is a current-based circuit. An op-amp is used to maintain equal voltages at the nodes V_A and V_B.

$$V_A = V_B = V_{BE,Q1} \tag{8}$$

Since $V_{BE,Q1}$ has a negative temperature dependence, a CTAT current flows across the resistors R_1 and R_2.

$$I_{R_2} = \frac{V_{BE,Q1}}{R_2} \tag{9}$$

On the other hand, a PTAT current flows across the resistor R_0.

$$I_{R_0} = \frac{V_{BE,Q1} - V_{BE,Q2}}{R_0} = \frac{\Delta V_{BE}}{R_0} \tag{10}$$

The difference in current densities is generated by using two diodes with different emitter areas. The ratio of biasing current is unity. The sum of the two currents should have a zero-temperature coefficient. The current mirror and the negative feedback loop around the op-amp force currents I_1 and I_2 to be equal. The CTAT and the PTAT currents are forced through the resistors R_2 and R_0 respectively.

$$I_1 = I_{CTAT} + I_{PTAT} = I_{R_2} + I_{R_0} \tag{11}$$

The ZTC current is achieved by using appropriate resistor values that ensure the cancellation of the temperature dependent components of each term. The ZTC current can be easily converted to a voltage by mirroring the current and forcing it through a resistor. The output reference voltage,

$$V_{ref} = I_1 R_3 = \frac{R_3}{R_2} V_{BE} + \frac{R_3}{R_0} \Delta V_{BE} \tag{12}$$

The Banba reference circuit was designed in IBM 130nm process and the temperature coefficient of the generated ZTC current was 17ppm/°C. The peak-to-peak current variation in the ZTC current was in the order of nano-amperes for a ZTC current, designed in the range of tens of micro-amperes.

2.2 Analysis of the Non-linear Component Causing Curvature

The curvature of the output is similar to Figure 3. As mentioned in Chapter 1, the curvature is caused by the non-linearity of V_{BE}. This is explained in this section. The temperature characteristics of the I_C-V_{BE} relations of bipolar junction transistors is explained by Tsividis equation [14]. It is rearranged as in (13)[15]. The detailed derivation of the temperature dependence of V_{BE} is presented in Appendix A.

$$V_{BE}(T) = V_{GOr} + \left(V_{BE}(T_r) - V_{GO,r}\right)\frac{T}{T_r} - (\eta)\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) + \left(\frac{kT}{q}\right)\ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \quad (13)$$

where T_r is the reference temperature and η is a process-dependent parameter. T_r is not a model parameter, but the expression is widely used in the analysis of bandgap-based references. If the collector current, $I_c(T) = DT^{\delta}$, where D is a constant [6] and δ is a constant defined by the temperature dependence of the collector current, the expression in (13) can be modified and re-arranged as in (14). In (13), V_{GO} (T) is approximated to have a linear temperature dependence ($V_{GO}(T) = V_{GOr} + €T$, where € is a temperature independent constant). $V_{GO}r$ is the extrapolated bandgap voltage at 0K. Hence (8) can be simplified as shown in (14)[15].

$$V_{BE}(T) = V_{GOr} + (V_{BE}(T_r) - V_{GOr})\frac{T}{T_r} - (\eta - \delta)\left(\frac{kT}{q}\right)\ln\left(\frac{T}{T_r}\right) \quad (14)$$

The Tln(T) term in (14) is the cause of curvature in the bandgap voltage reference circuit.

A PTAT voltage can be generated by as explained in (10).

$$V_{BE1}(T) - V_{BE2}(T) = \frac{T}{T_r}\left(V_{BE1}(T_r) - V_{BE2}(T_r)\right) \quad (15)$$

$V_{BE1}(T_r)$ and $V_{BE2}(T_r)$ are the base-emitter voltages across the bipolar junction transistors at the reference temperature and are considered as temperature-independent constants. From Figure 4 it is understood that a current proportional to the voltage in (15) flows through the diodes Q1 and Q2 and is PTAT in nature, while a CTAT current, corresponding to the voltage in (14) flows through the resistors R1 and R2. The sum of the two currents flows through the current mirror transistors N_1 and N_3 and is ZTC is nature. From (14) and (15), it is also evident that the BGR circuit tends to cancel the first-order temperature dependent term while the higher order Tln(T) term remains, causing the curvature.

For many standard applications, performance at the level of a few tens of ppm/°C (achieved by first-order reference circuits) is desired and much better performance is required in other applications, presenting a need for curvature compensation. Various curvature compensation techniques have been researched in the past. A few methods are explained in Chapter 4.

CHAPTER 3: NON-IDEAL EFFECTS AFFECTING THE PERFORMANCE

In this chapter, various non-idealities and parasitic effects that affect the performance of a bandgap reference circuit are described. A few parasitic effects are complex and challenging to model. Most of the low-cost CMOS processes fail to model the temperature-dependencies of non-idealities such as current gain, base resistance, non-ideality factor etc. Hence, the simulations do not capture the effect of these non-idealities. Various sources of errors and their contributions have been discussed in [16].

As explained earlier, low cost CMOS processes have parasitic BJTs which are used for generating the required voltages. The BJTs are configured as diodes by connecting the base and collector. There are two types of parasitic transistors: Lateral BJTs and Vertical/Substrate BJTs as shown in Figure 5.

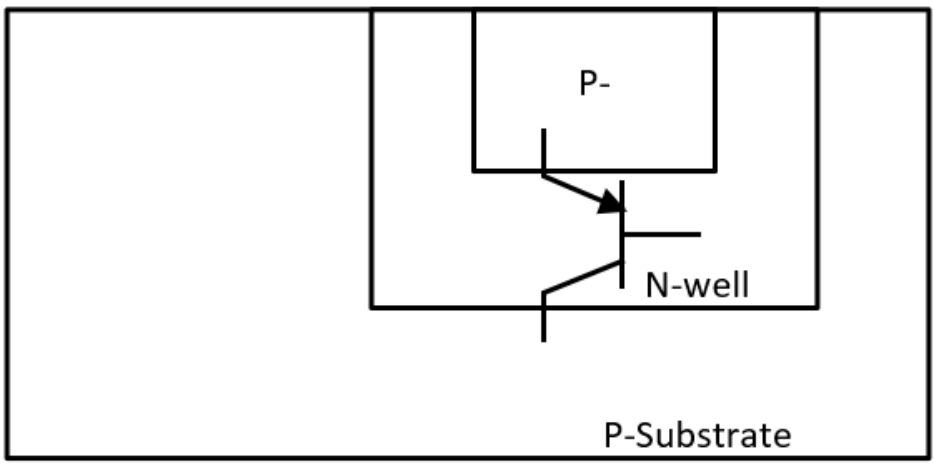


Figure 5 : Substrate PNP in a CMOS-process

Lateral BJTs are seldom used in the implementation of voltage reference circuits. This is because a lateral bipolar junction transistor has an associated vertical bipolar junction transistor. A portion of the biasing emitter current of the lateral BJT is forced through the vertical BJT, instead of its collector. Hence, it is limited to configurations where the

transistor is biased at the collector end and the relationship is no longer exponential [17]. The substrate PNP transistors, with grounded collector terminal/ substrate is most widely available. The P^+ diffusion/N-well form the emitter/base terminals respectively. There are a few CMOS processes that offer vertical NPN transistors, mostly created by a Deep N-well/P-well/N-diffusion corresponding to collector/base/emitter respectively.

The subsequent parts of this chapter enlist primary error sources and other parasitic effects that determine the maximum achievable performance of the bandgap circuit.

3.1 Error Sources and Parasitic Effects

3.1.1 Op-amp Offset

From Figure 4, it can be observed that an op-amp is used to maintain $V_A = V_B$. There is a finite offset voltage associated with the op-amps.

$$V_{BE1}(T) = V_{BE2}(T) + Vos \tag{16}$$

$$V_{PTAT} = V_{BE1}(T) - V_{BE2}(T) - Vos \tag{17}$$

From (17), it can be analyzed that V_{PTAT} is no longer truly PTAT in nature. It is a significant source of error in the bandgap reference circuit performance[16]. Additionally, there is an associated offset voltage drift with temperature, which affects the performance.

One of the techniques used to reduce the offset voltage-related effects is the use of chopper-stabilized or auto-zero amplifiers which have ultra-low offset voltages and a zero-drift performance. Chopper amplifiers can achieve a low offset voltage in the order of a few micro-volts and the offset drift in the nV/°C range. For low power applications, where the biasing current is smaller in magnitude, the bias current of the op-amp becomes significant.

3.1.2 Current Gain and Base Current

The current gain of a BJT is defined as the ratio of the collector current, I_C and the base current I_B.

$$\beta = \frac{I_C}{I_B} \tag{18}$$

β is a process dependent parameter. In true bipolar processes, the bipolar transistors have a current gain in the order of 100's. This implies that when a BJT is biased at the collector end, the base current is minimal.

But the parasitic bipolar junction transistors in most of the CMOS processes have a current gain in the range of 1-10. Since the collector is the substrate and hence grounded, the transistors are biased at the emitter end and (18) can be modified and rearranged in terms of emitter current as follows.

$$I_C = \frac{\beta}{1+\beta} I_E \tag{19}$$

When biased at the emitter end (for a diode-connected configuration), there would be an appreciable base current, which flows through the base resistance (described in the following section) contributing to an error voltage in the V_{BE}. The current gain depends on the bias current, temperature and layout of the transistors.

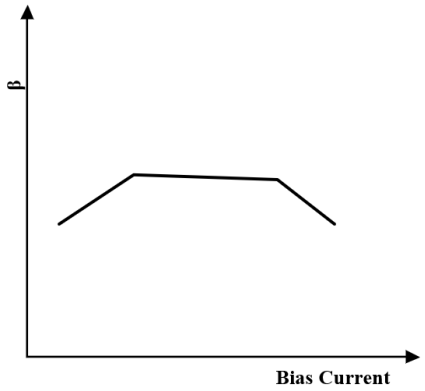


Figure 6 : Current gain Vs Bias current

The dependency of current gain β on the biasing current is shown in Figure 6**.** β is low for low magnitudes of biasing currents, rises and stays constant over a range of biasing currents and subsequently drops for very high values of emitter currents. At very low biasing currents, the recombination at the emitter-base junction becomes significant, thereby contributing to low β. At high values of emitter currents, high level injection becomes significant.

The Gummel-Poon model, which is the classic model used for bipolar junction transistors, defines the temperature dependency of current gain as

$$\beta(T) = \beta_O \left(\frac{T}{T_O}\right)^{XTB} \tag{20}$$

where $\beta(T)$ is the current gain at temperature T, β_O is the current gain at temperature T_O, which is the nominal temperature and XTB is the forward or reverse temperature coefficient of β. From (20), it can be understood that β increases with increase in temperature[18]. It is desirable to choose the biasing emitter currents in the region where β remains constant.

Most of the available CMOS processes do not model the temperature dependency of β and XTB is set to 0. This makes it hard for analyzing the effect in simulation. The Tsividis equation in (13) can be modified as (21)[18] based on (19) and (20) and the temperature dependence of current gain, contributes to an error.

$$V_{BE}(T) = V_{GOr} + (V_{BE}(T_r) - V_{GOr})\frac{T}{T_r} - (\eta - \delta)\left(\frac{kT}{q}\right)\ln\left(\frac{I_E(T)}{I_E(T_r)}\right)$$

$$+ (\eta - \delta)\left(\frac{kT}{q}\right)\ln\left(\frac{\beta(T)(1+\beta(Tr)}{\beta(T_r)(1+\beta(T)}\right) \tag{21}$$

3.1.3 Base Resistance

Base resistance is a significant non-ideality that affects the performance of the bandgap circuit. The base region of the transistor, normally the N-well, in case of a PNP transistor, has an appreciable base resistance. The voltage drop across the base resistance contributes to an error voltage term. Let $V_{BE,true}$ be the ideal base-emitter voltage, that is explained in (13).

$$V_{BE} = V_{BE,true} + I_B R_B$$

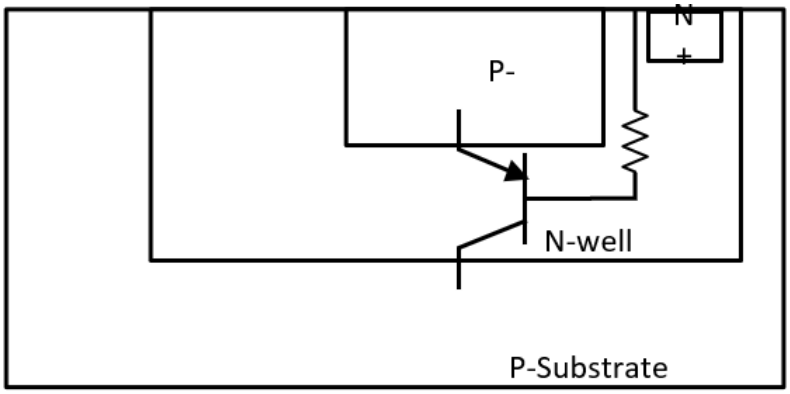


Figure 7 : Base resistance

The base resistance is found to be dependent on the number of contacts in the base, the distance between the emitter and base, the width of the base etc. Multi-emitter geometry with multiple base-contacts in between can help reduce the base resistance. This may increase in the base current, hence establishing a trade-off between the two parameters. Lowering the biasing emitter current reduces the base current value but increases the noise and interference in the system.

CHAPTER 4:STATE-OF-THE-ART CURVATURE CORRECTION TECHNIQUES

4.1 Principle of Curvature Compensation

As explained in the previous chapters, the principle of a first-order bandgap circuit is the same and is supported with mathematical equations. Now, the objective is to cancel the higher order non-linear terms in V_{BE} (T) to achieve a perfectly flat output. In most of the circuits, this is achieved by generating a non-linear term and using it to cancel the non-linearity in $V_{BE}(T)$.

Another aspect that needs to be considered is that most of the existing curvature correction circuits neglect the effect of many non-ideal factors described in Chapter 3. The simulation results are limited by the accuracy of the models used. The effect of package shifts also imposes a challenge to high accuracy.

4.2 Existing Curvature Compensation Techniques

This section describes a few curvature compensation schemes among the many strategies that have been implemented.

4.2.1 Squared-PTAT Curvature Correction

A commonly used method for curvature compensation involves the addition of a squared PTAT term to the existing first-order bandgap reference circuit output, which essentially helps to cancel the second order non-linearity in the V_{BE} term[19]. From the Taylor series expansion of Tln (T) term, it can be observed that the contribution towards the non-linearity decreases from the first-order to the higher-order terms. Since the first-order bandgap circuits tend to cancel the first-order temperature dependency, the target is to cancel the higher order terms. This approach involves the cancellation of the second order term and

leave behind the higher order terms. Figure 8 shows an illustration of the curvature compensation using this method in the Brokaw bandgap reference circuit[6].

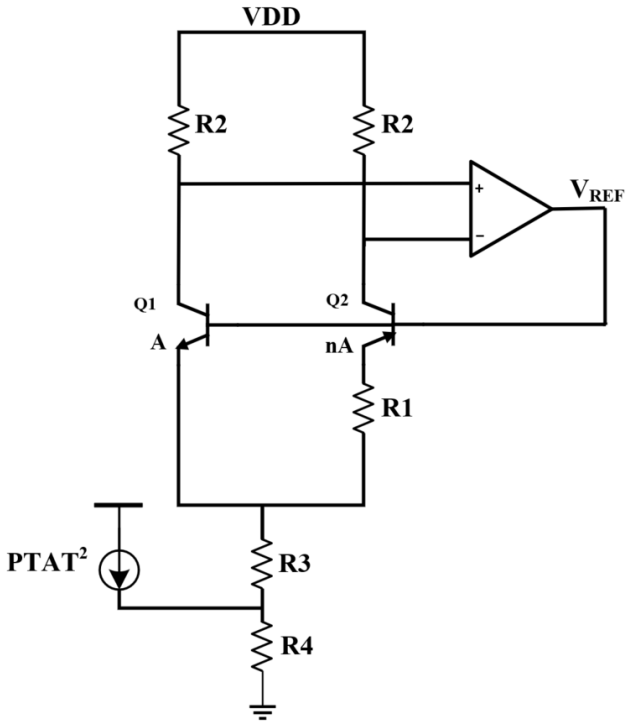


Figure 8 : Curvature compensated circuit using squared PTAT current

Assuming that the op-amp is ideal, the currents that flow through the transistors Q1 and Q2 are PTAT in nature. An additional $PTAT^2$ current generator is used to force current through the resistor R_4.

The curvature compensated voltage reference output can be expressed as

$$V_{REF} = V_{BE2} + I_{PTAT}(R_1 + 2R_3 + R_4) + I_{PTAT^2}R_4 \quad (21)$$

At the lower temperature range, the first-order temperature dependent $(V_{BE} + V_{PTAT})$ term is dominant. As the temperature increases, the $PTAT^2$ term becomes dominant and hence, the higher order non-linearity in V_{BE} is cancelled using its quadratic behavior. A typical profile of second-order curvature compensated reference circuits is shown in Figure 9.

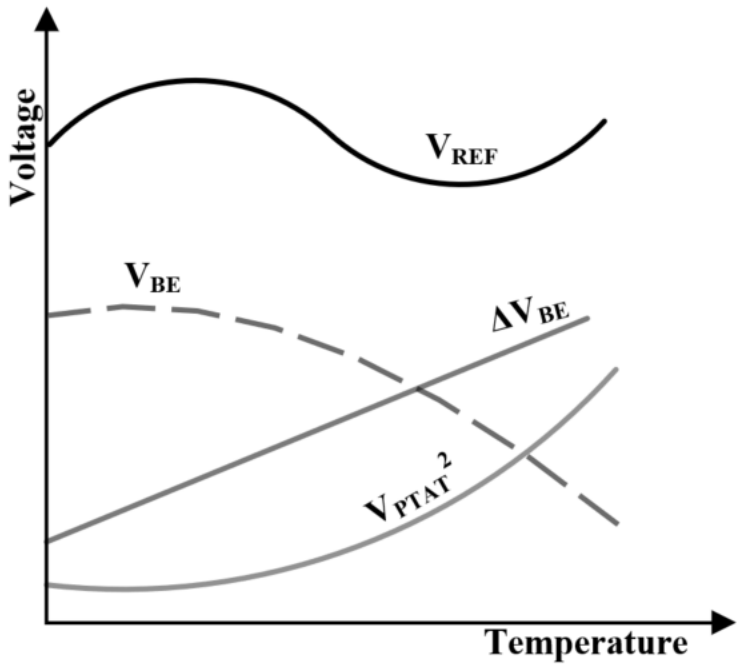


Figure 9 : Profile of the curvature compensated output

It can be observed that the remaining terms in the logarithmic expansion of V_{BE} (the third-order term and the higher order non-linear terms) are left uncompensated and the output profile is dominated by the third-order behavior.

4.2.2 Diode Loop Curvature Correction

Another technique for curvature compensation requires the use of temperature-dependent currents and a diode-voltage loop[6] [21].The circuit uses a current-based compensation technique. The idea is to generate a non-linear current, I_{NL} which is designed to cancel the higher order curvature component of V_{BE} (T) term. If the non-linear term is compensated, V_{GOr} and the first-order terms are left in V_{BE} expansion. The first-order term can be easily cancelled by using a PTAT current generator.

A conceptual implementation of the circuit[6] is presented in Figure 10**.**

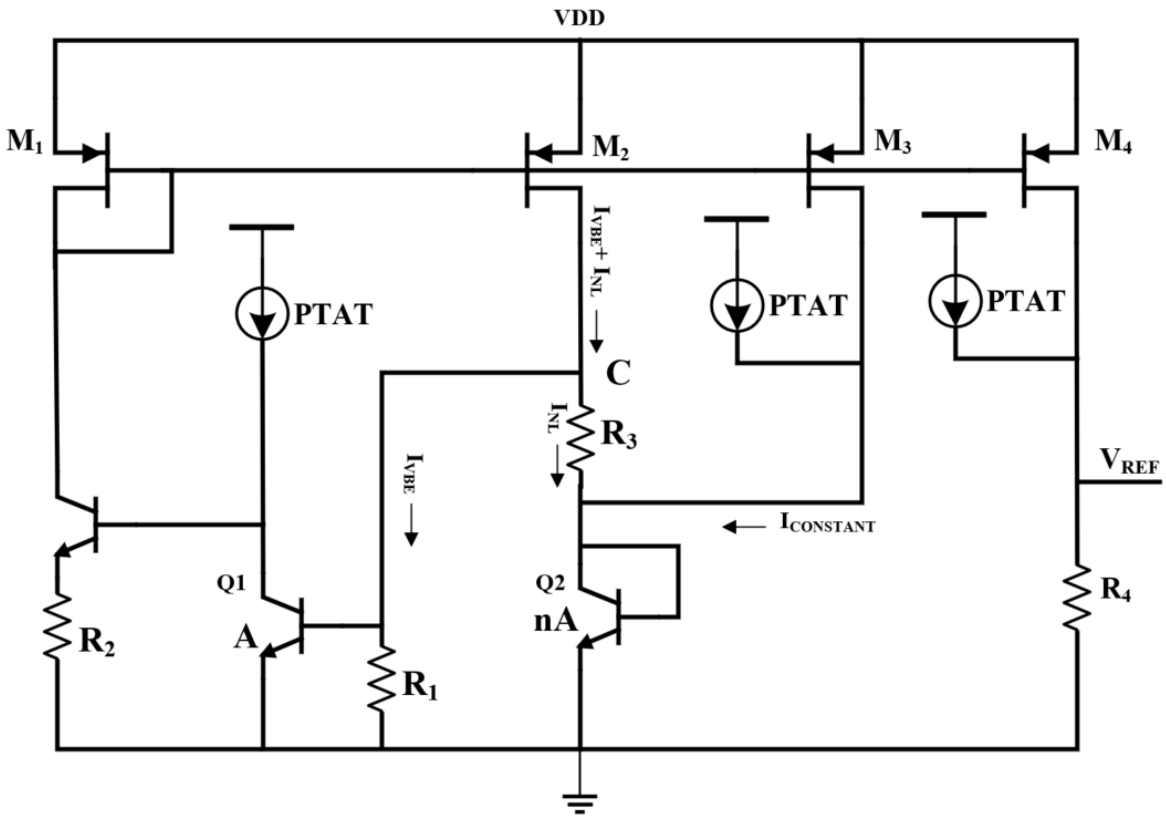


Figure 10 : Diode loop curvature correction method

The circuit explains a dynamic curvature compensation scheme. The circuit is designed such that a non-linear current is forced across resistor R_3.

$$I_{VBE} = \frac{V_{BE1}}{R_1} \tag{22}$$

where V_{BE1} is the base-emitter voltage across transistor Q_1, when biased by a PTAT current.

$$I_{NL} = \frac{V_{BE1} - V_{BE2}}{R_3} \tag{23}$$

$$= \frac{V_T}{R_3} \ln\left(\frac{I_{C1}A_2}{A_1 I_{C2}}\right)$$

$$= \frac{V_T}{R_3} \ln\left(\frac{nI_{PTAT}}{I_{NL} + I_{CONSTANT}}\right)$$

It can be observed that I_{NL} is a logarithmic function of itself and its non-linear property is used to cancel the higher order non-linearity of V_{BE}. The current mirror circuit is forced to generate a current that is equivalent to the sum of I_{VBE} and I_{NL}, by utilizing a feedback loop. At node C, I_{VBE} is forced through resistor R_1 and I_{VNL} is forced through resistor R_3.

At the third leg of the circuit, a constant current is generated that equals the sum of the three-temperature dependent currents in the circuit.

$$I_{CONSTANT} = I_{VBE} + I_{PTAT} + I_{NL} \tag{24}$$

$$= \frac{V_{BE1}}{R_1} + I_{PTAT} + \frac{V_{NL}}{R_3}$$

$$\approx \frac{V_{GOr}}{R_1}$$

The resistors R_1 and R_3 are chosen to cancel the desired temperature dependencies. I_{PTAT} is designed to cancel the first-order temperature term in V_{BE1}.

The feedback network will force the appropriate current across each leg of the circuit and the circuit becomes stable. Once this has been established, the voltage reference can be generated by accurately mirroring the sum current and PTAT current, thereby generating the constant current and forcing it through a resistor R_4.

$$V_{REF} = I_{CONSTANT} R_4 \tag{25}$$

$$\approx \frac{V_{GOr} R_4}{R_1}$$

This concept of dynamic curvature compensation is slightly complicated and is prone to errors introduced by the non-ideal effects, the temperature coefficient and accuracy of the associated resistors used for cancellation and the mismatch between the current mirrors. The additional circuitry for PTAT current generation makes the circuit area intensive.

4.3.3 Exponential Curvature Compensation

The technique utilizes the temperature dependence of the current gain, β, explained in Chapter 3 for curvature compensation[19].

$$\beta \alpha e^{-1/T} \tag{26}$$

A simple illustration of the concept is shown in Figure 11[6]**.** The circuit uses two PTAT current sources. The voltage reference output V_{ref} can be expressed as

$$V_{REF} = -R\left(AT + \frac{BT}{\beta}\right) - V_{BE} \tag{27}$$

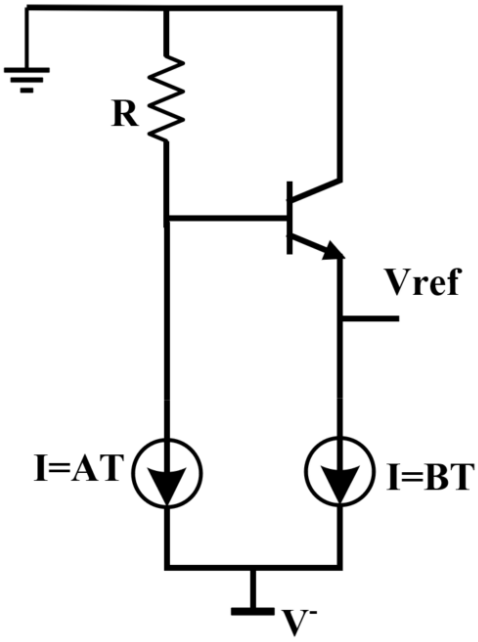


Figure 11 : Exponential curvature compensation

The term $\frac{BT}{\beta}$ represents the effect of the base current of the BJT, causing a voltage drop across the resistor. The coefficient A and B are designed to generate the first-order and the non-linear term required for curvature cancellation. Since β is dependent on the bandgap narrowing factor, the technique is found to be process dependent. It does not require any additional circuitry and has a simple implementation.

CHAPTER 5: ADOPTED METHOD OF V_{GO} EXTRACTION

5.1 Modified Expression for V_{BE}

Before the concept of extraction is explained, it is imperative to discuss a few assumptions, which introduce errors in the existing analysis and propose suitable modifications. The Tsividis equation, in (14) follows the assumption that the bandgap voltage, V_G (T) varies linearly with temperature, which may not necessarily be true. The temperature dependence of bandgap voltage is represented by the non-linear expression[14] in (28).

$$V_G(T) = V_{GO} - \frac{\alpha T^2}{T + \beta} \tag{28}$$

where α and β are constants and V_{GO} is the bandgap voltage of Silicon at 0K. V_{GO} is a physical constant and is inherently not dependent upon any process parameters, and if a circuit could be designed that expresses V_{GO} at the output, the circuit would serve as an ideal voltage reference.

Figure 12 shows the difference between the linear approximation of the bandgap voltage and the actual bandgap voltage, plotted over a range of temperatures.

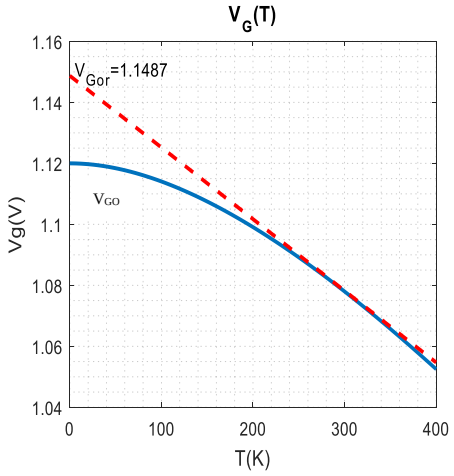


Figure 12: V_G(T) and the error introduced by linear approximation

From Figure 12, it is evident that the actual bandgap voltage at 0K, V_{GO} is not equal to the extrapolated bandgap voltage at 0K, V_{GOr} used in (14). Hence, a modified expression for V_{BE} is presented in terms of the V_{GO}.

Using the basis function, the bandgap voltage of Silicon can be expressed as (29).

$$V_G(T) = V_{G0} + a' T + b' T\ln(T) + \varepsilon(T) \tag{29}$$

where a', b' are the regression coefficients and $\varepsilon(T)$ is the residual error term.

$$V_G(T_r) = V_{G0} + a' T_r + b' T_r\ln(T_r) + \varepsilon(T_r) \tag{30}$$

Using (29)-(30), a modified expression for V_{BE} is derived as (31).

$$V_{BE}(T) = V_{GO} + \varepsilon(T) + \left(\frac{T}{T_r}\right)(V_{BE}(T_r) - V_{GO} - \varepsilon(Tr)) - \eta\frac{kT}{q}\ln\left(\frac{T}{T_r}\right) + b' T \ln\left(\frac{T}{T_r}\right) + \frac{kT}{q}\ln\left(\frac{I_C(T)}{I_C(T_r)}\right) \tag{31}$$

If the collector current is proportional to T^{δ}, (31) can be rearranged and modified as

$$V_{BE}(T) = V_{GO} + \varepsilon(T) + \left(\frac{T}{T_r}\right)(V_{BE}(T_r) - V_{GO} - \varepsilon(Tr)) - ((\eta - \delta)\frac{k}{q} - b')T \ln\left(\frac{T}{T_r}\right) \tag{32}$$

5.2 Non-Linear Term Generation

The principle of curvature compensation has been described in Chapter 4. Here, an approach is made to cancel the non-linear components in V_{BE} (T), by generating a non-linear term, proportional to Tln(T) [22] using temperature-dependent currents.

Consider the base-emitter voltages across two diode-connected transistors biased by a PTAT current and a temperature independent current respectively as shown in Figure 13**.** The base-emitter voltages across the two diodes can be expressed as (33) -(34).

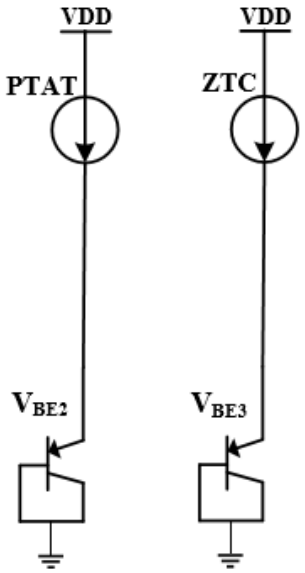


Figure 13: Set up for Non-linear Voltage Generation

$$V_{BE2}(T) = V_{GO} + \varepsilon(T) + \left(\frac{T}{T_r}\right)(V_{BE2}(T_r) - V_{GO} - \varepsilon(Tr)) - ((\eta - 1)\frac{k}{q} - b')T\ln\left(\frac{T}{T_r}\right) \quad (33)$$

$$V_{BE3}(T) = V_{GO} + \varepsilon(T) + \left(\frac{T}{T_r}\right)(V_{BE3}(T_r) - V_{GO} - \varepsilon(Tr)) - ((\eta - 0)\frac{k}{q} - b')T\ln\left(\frac{T}{T_r}\right) \quad (34)$$

The non-linear term, V_{NL} can be expressed as

$$V_{NL} = V_{BE3}(T) - V_{BE2}(T) = \left(V_{BE3}(T_r) - V_{BE2}(T_r)\right)\left(\frac{T}{T_r}\right) - \frac{k}{q}T\ln\left(\frac{T}{T_r}\right) \quad (35)$$

The term $V_{BE3}(T_r) - V_{BE2}(T_r)$ is ignored in [22] following an incorrect assumption that $V_{BE3}(T_r) = V_{BE2}(T_r)$. To generate a non-linear term proportional to Tln(T), the circuit should be designed such that at the reference temperature T_r, the base-emitter voltages are equal and cancel each other.

$$V_{NL} = \left(-\frac{k}{q}\right)T\ln\left(\frac{T}{T_r}\right) \quad (36)$$

5.3 V_{GO} Extraction

The proposed method targets the extraction of V_{GO} and its expression at the output of a voltage reference circuit, in contrast to the existing curvature-compensation circuits that focus on cancelling the non-linearity in V_{BE}. Figure 13 depicts three diode-connected PNP transistors, Q1, Q2 and Q3, out of which Q2 and Q3 have the same emitter area and Q1 has a larger emitter area. The transistors are biased by currents I_1, I_2 and I_3 such that I_1 and I_2 are PTAT in nature and I_3 have a zero-temperature coefficient (ZTC).

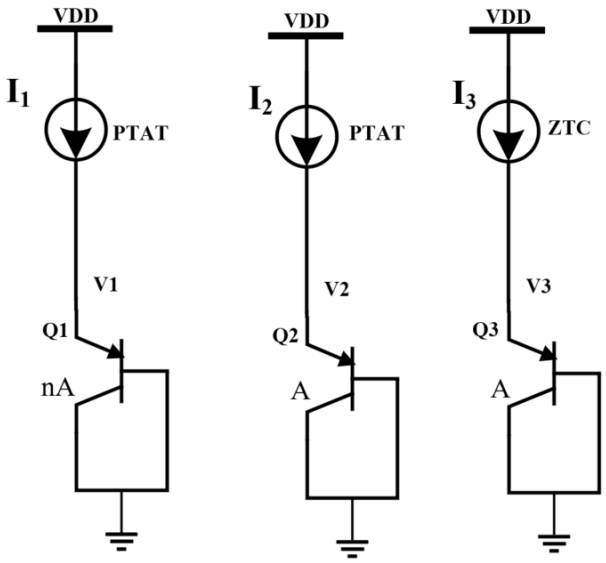


Figure 14 : Voltage generation

Now, a PTAT voltage, V_{PTAT} and a non-linear voltage V_{NL} are generated as in (3).

$$V_{PTAT} = V_{BE2}(T) - V_{BE1}(T) = (V_{BE2}(T_r) - V_{BE1}(T_r))\left(\frac{T}{T_r}\right) \quad (37)$$

For simplicity, (33), (36) and (37) can be expressed as follows,

$$V_{BE} = V_{GO} + \varepsilon(T) + aT + bT\ln(T) \quad (38)$$

$$V_{NL} = cT\ln(T) \quad (39)$$

$$V_{PTAT} = dT \quad (40)$$

where a, b, c and d are temperature independent terms after re-arranging (33), (36) and (37).

If a linear recombination of V_{BE}, V_{PTAT} and V_{NL} is performed such that the linear (T) and non-linear (TlnT) terms get cancelled, then V_{GO} can be expressed at the output and the resultant reference voltage achieves a very low temperature coefficient.

$$V_{ref} = A_1V_{BE} + A_2V_{NL} + A_3V_{PTAT} \approx V_{GO} + e(T) \quad (41)$$

where e(T) is the cumulative error term, which includes the residual terms $\varepsilon(T)$, noise etc. It is small in magnitude and is neglected in the analysis.

The task involves the determination of the coefficients A_1, A_2 and A_3 which will be in terms of the temperature-independent terms, a, b, c and d described above.

Using (38)-(40), (41) can be re-arranged as

$$V_{ref} = V_{GO}(A_1) + T\ln(T)(b + cA_2) + T(a + A_3d) \quad (42)$$

The desired output voltage is V_{GO} and hence, the coefficients of all the temperature dependent terms can be equated to zero to obtain the desired coefficients in (41).

$$A_1 = 1 \quad (43)$$

$$A_2 = -\frac{b}{c} \quad (44)$$

$$A_3 = -\frac{a}{d} \quad (45)$$

Once the constant coefficients are determined, (41) needs to be accurately realized to achieve the desired performance. The equation can be implemented using a suitable analog/digital circuitry. A summing/difference amplifier, using resistors may be used to implement (41). Alternatively, an analog-to-digital converter (ADC) may be used to convert the voltages into digital signals, which can be processed using a digital signal processor (DSP) and later converted back to analog domain using a digital-to-analog converter (DAC). This thesis mainly focuses on the analog domain implementation using resistors.

5.4 Design of the Current Sources

Determining the coefficients require the voltages across the diodes when biased by appropriate currents. The extraction procedure requires a ZTC current and a PTAT current. The ZTC current may be generated using any of the first-order bandgap reference circuits shown in Figure 2. A Banba circuit explained in Chapter 2 was designed in UMC-65nm process as shown in Figure 15.

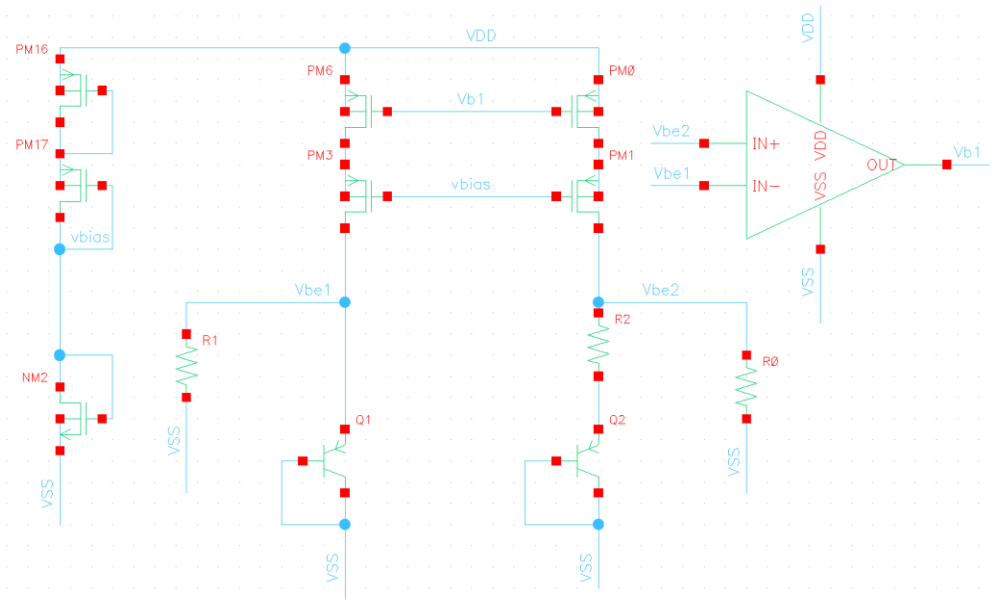


Figure 15 : Banba circuit designed in UMC 65nm process

Two diode-connected bipolar junction transistors, in the ratio 2:12, having an emitter size 2u x 2u, are utilized for generating the appropriate temperature dependent currents. The resistors are designed to cancel the first-order temperature dependencies and scaling the resistors can shift the inflection point (the temperature at which the derivative is zero). A SPICE model of a chopper/zero-drift amplifier, ADA4528 was used to maintain Vbe1 = Vbe2 and set the voltage, V_{b1}. The systematic offset is modelled while the offset drift is not modelled in the SPICE model. Hence, any temperature-based effects associated with the op amp cannot be captured in simulations. The voltage V_{bias} is set by an appropriate voltage bias circuitry using MOSFETs as shown. A single supply configuration was used in the design. Cascoded current mirrors were used to ensure V_{DS} matching for the current mirror circuits.

The circuit was designed to generate a current having a temperature coefficient of 12.45 ppm/°C in the temperature range of -40°C to 125°C and the profile of the temperature independent current is shown in Figure 16. The peak-to-peak variation is approximately 23nA for an 11.3uA reference current.

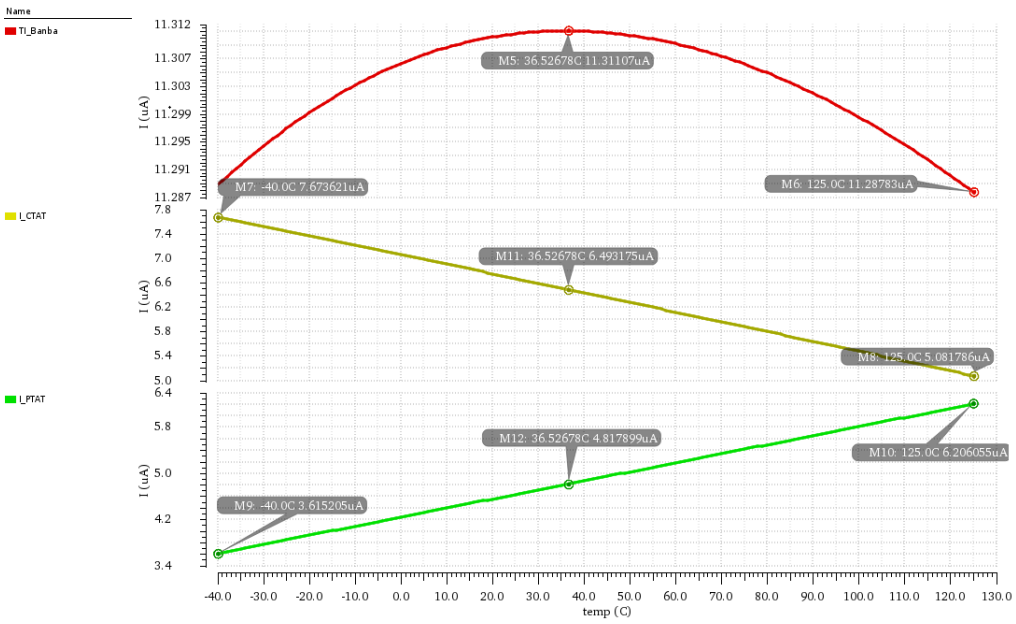


Figure 16 : ZTC current, CTAT current and PTAT current profiles

The current can be converted to a voltage by forcing through a resistor. The voltage profile of the output is shown in Figure 17. The peak to peak voltage variation of the output voltage over the entire temperature range is approximately 2mV for a 1V reference output.

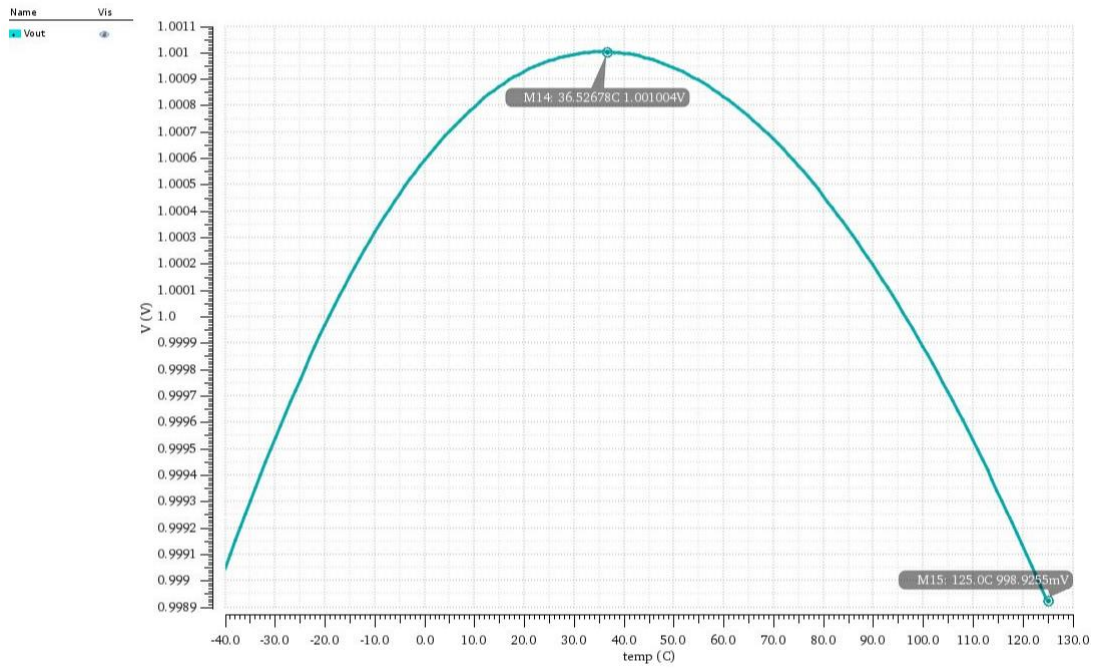


Figure 17 : Output voltage of a first-order bandgap reference circuit

A conventional PTAT current source[23] was designed in UMC-65nm process for generating the PTAT current as shown in Figure 18.

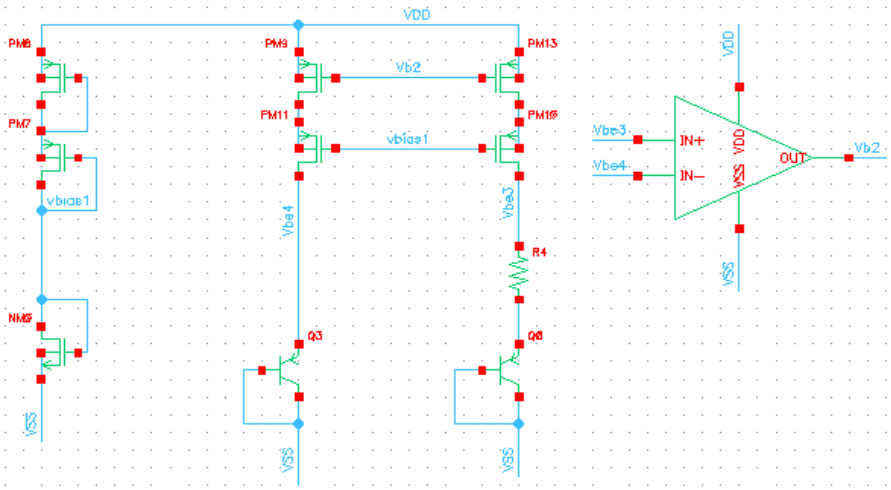


Figure 18 : PTAT current generator

The profile of the current is presented in Figure 19. The working of the circuit can be explained using the operation of Banba circuit discussed in Chapter 2. In Figure 15, CTAT current flows through the resistors R_1 and R_2, while PTAT current flows through resistor R_0. If the resistors R_1 and R_2 are removed, the current mirror transistors generate the PTAT current described in (10), which flows through R_0. Like the Banba circuit, a chopper amplifier maintains the voltages $V_{be3} = V_{be4}$ and sets the voltage at the node V_{b2}. The resistor value is chosen to generate a current of 11.3uA at 27°C.

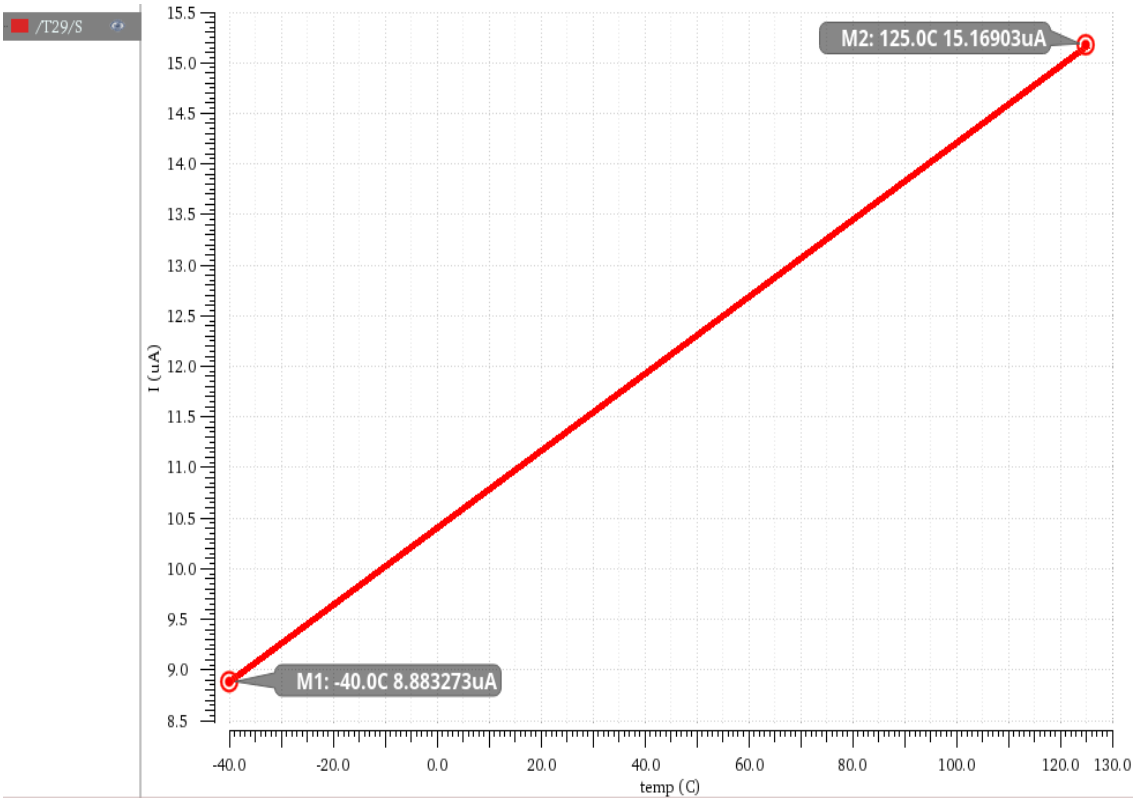


Figure 19 : Current output of the PTAT current generator

The currents are mirrored and used to bias the three diode-connected transistors shown in Figure 14. Q1 and Q2 have an emitter area of (2u x 2u) with a multiplier 2 while Q3 has the same emitter area with a multiplier 12. The PNP diodes are comprised of the

P+/N-well/P-substrate which forms the emitter, base, collector respectively. The layout associated with the parameterized cell in the process is shown in Figure 20.

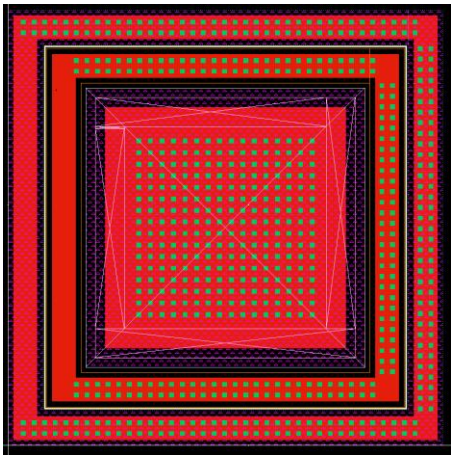


Figure 20: P-cell layout for a PNP transistor with emitter area 2u x 2u

5.5 Voltage Term Generation

The voltage terms, V_{BE}, V_{NL} and V_{PTAT} need to be generated after suitably biasing the transistors. An ideal voltage-controlled voltage source (VCVS) in the analogLib library set to unity gain is used to generate the difference terms described in (35) and (37) as shown in Figure 21.

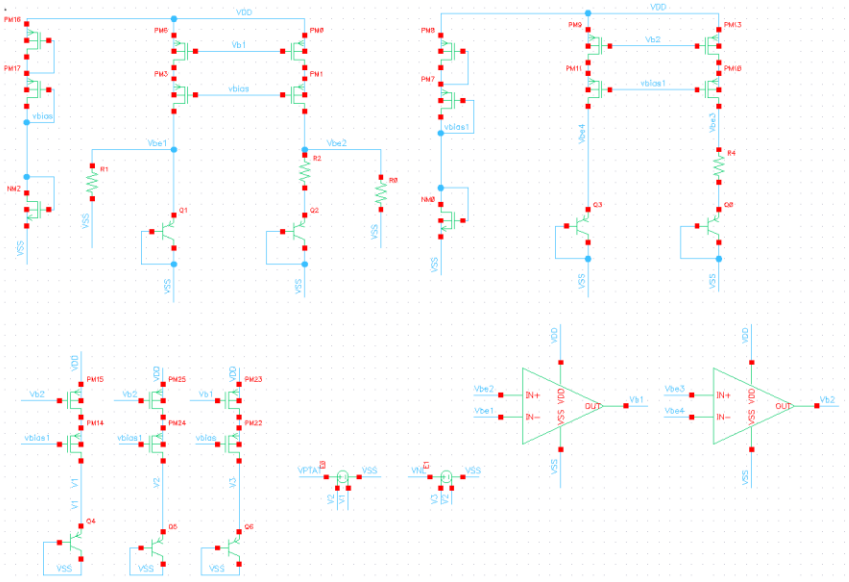


Figure 21 : Schematic for voltage term generation

5.6 Coefficient Determination

5.6.1 Generating the Coefficients Using Derived Equations

The coefficients A_1, A_2 and A_3 need to be determined. The coefficients can be determined mathematically using (43)-(45), but the parameter 'b' of (44) has an unknown term b' (29). All the remaining terms are physical constants, except η, which is a process dependent and temperature-independent parameter. The actual value of V_{GO} is unknown as in Figure 12. Hence, using the equations (43)-(45) cannot be used to determine the coefficients for curvature cancellation.

5.6.2 Generating the Coefficients Using Fitting Approach

Another approach involves utilizing the measured base-emitter voltages at different temperatures for determining the coefficients. Since the equations can't be used due to the unknown parameters, the base-emitter voltages recorded at two or more temperatures is required for the process.

The task is to utilize a range of base-emitter voltages (from simulation) across the desired temperature range, for determining the appropriate coefficients A_2 and A_3 such that the resultant reference may have a lower temperature coefficient. The voltages V_{PTAT} and V_{NL} are generated in simulation, as described in section 5.5. This process essentially evolves to a fitting procedure, as described below.

Since the desired temperature range of operation is -40°C to 125°C, the voltages V_{BE}, V_{PTAT} and V_{NL} recorded at 1°C intervals are utilized, resulting in a system of 166 equations and two unknowns, A_2 and A_3. The set of equations can be considered as an over-determined system, i.e. a system that has more equations than unknowns and is, mostly inconsistent.

However, an approximate solution may be determined by using least square method. This method provides a solution that best fits the given set of equations. The optimum value

of the unknown parameter is calculated such that the squared-sum of the errors between the actual output and the value predicted by the least square model is minimized.

Since least square analysis may be easily performed in MATLAB, all the required voltage values are exported from Cadence to MATLAB. There are 3 sample data sets in MATLAB, each consisting of 166 points corresponding to V_{BE}, V_{PTAT} and V_{NL}. Since the coefficient A_1 is set to unity, (42) may be rearranged for ease of analysis.

$$V_{ref} = V_{BE} + A_2 V_{NL} + A_3 V_{PTAT} \quad (46)$$

Now, the coefficient A_2 and A_3 that best fits the above equation is determined by least square analysis in MATLAB after setting V_{GO} = 1.1487V. Here, V_{GO} is set equal to V_{GOr}, the extrapolated bandgap voltage of silicon at 0K shown in Figure 12.

The coefficient values were obtained as

A_2 = -2.1032

A_3 = 10.0914

After substituting the coefficient values in (42), the output reference voltage was generated using ideal components as shown in Figure 22.

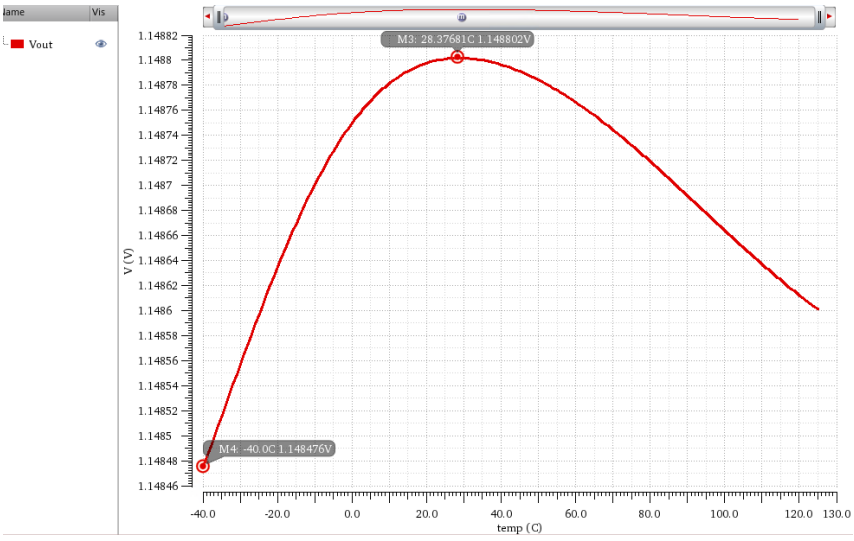


Figure 22 : Output after two-coefficient determination using least square method

The temperature coefficient is 1.718 ppm/°C. An interesting observation is that while the expected profile of the curvature compensated output is similar to a third-degree equation as explained in Chapter 4, the output profile is similar to that of a Banba reference circuit, which is a first-order reference circuit. The peak-to-peak output voltage variation is 326uV for a 1.14V output, which is much smaller than the 2mV peak-to-peak output voltage variation obtained in the Banba reference output. This analysis indicates curvature cancellation but there is significant non-linearity, left uncompensated in the system that prevents the circuit from achieving sub-ppm/°C temperature coefficient. It is interesting to observe that if the output voltage profile is evaluated at temperatures higher than 125°C, a profile similar to the third-order system is be obtained.

In order to debug this, the output reference voltage is decomposed into its constant, linear (T-T_r term) and non-linear ($(T - Tr)\ln\left(\frac{T}{Tr}\right)$) components. These terms are generated in MATLAB forming 3 matrices having 166 points each. A least square analysis is performed between the three matrices and the output reference voltage as shown in Figure 23.

```
base1 = ones(size(T));                          % constant

Tr = 29 +273;

base2 = T-Tr;                                   % linear

base3 = (T-Tr).*log((T)/(Tr));                  % non-linear

base = [base1 base2 base3];

a = base\Vref_calc1;

subplot(4,1,1) ; plot(T, base1*a(1)); title ('Vout constant term') ;

subplot(4,1,2) ; plot(T, base2*a(2)); title ('Vout linear term') ;

subplot(4,1,3) ; plot(T, base3*a(3)); title ('Vout non-linear term') ;

subplot(4,1,4) ; plot(T, Vref_calc1 - base*a); title ('Vout residual term')
```

Figure 23 : MATLAB code for decomposition

The components are plotted after multiplying the three terms with the appropriate least square coefficients. After fitting, the higher order residual terms contribute to an error obtained by subtracting the original output and the fitted output. The reference temperature is taken as 29°C.

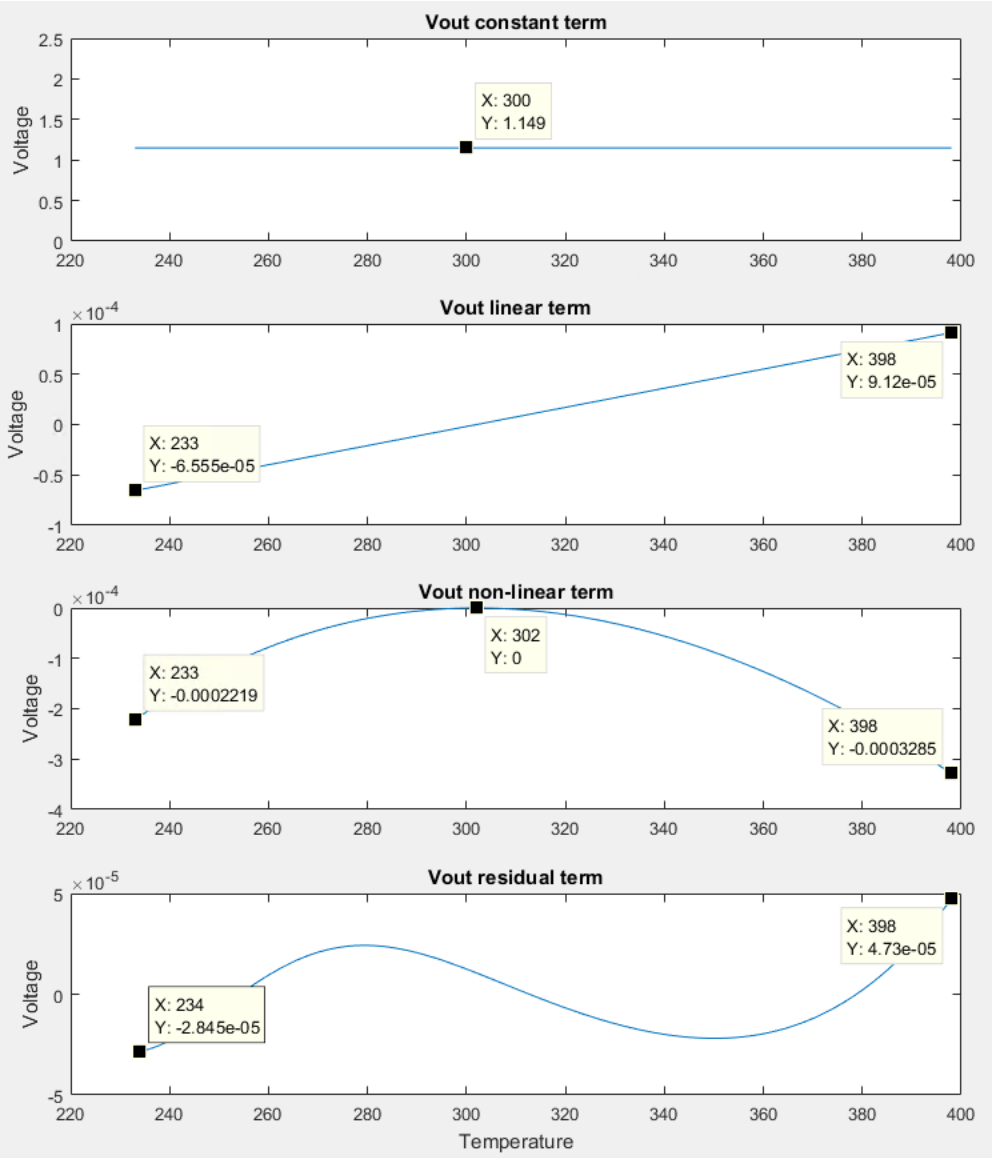


Figure 24 : Decomposition of the output after linear recombination

From Figure 24, it can be observed that in the output decomposition, the constant part is 1.149V, which is expected. The peak-to-peak variations are in the order of 156uV for the

linear term, 328uV for the non-linear component and 75uV for the residual term. The major contribution is from the non-linear term.

In order to isolate the source of non-linearity in the output, all the remaining voltage components are decomposed.

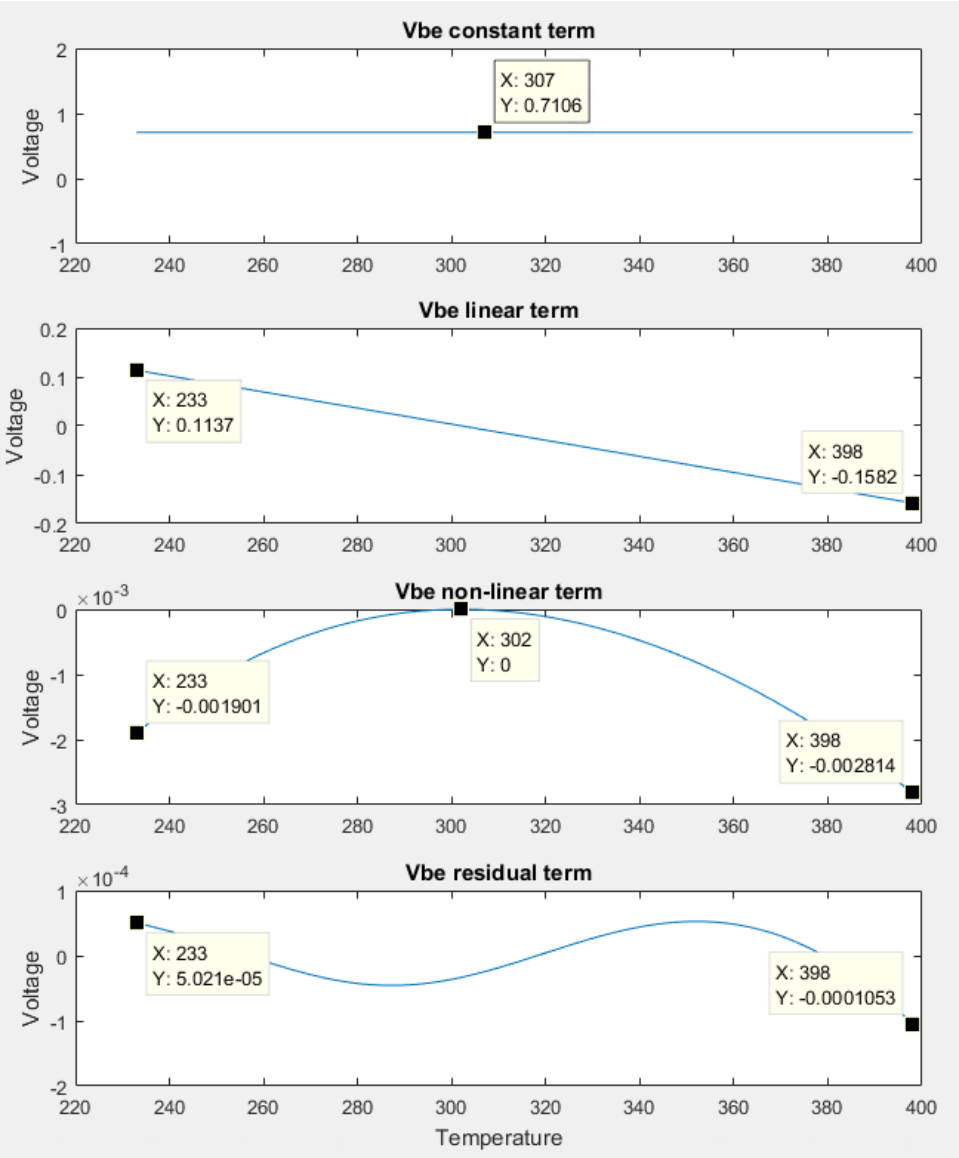


Figure 25 : Decomposition of V_{BE} component

The V_{BE} term has a constant component of 710mV. The peak-to-peak variations are in the order of 271mV for the linear term, 2.8mV for the non-linear term and 55uV for the

residual terms. The linear term is compensated by the PTAT voltage term and the remaining variation is being targeted for compensation.

After multiplying with the corresponding least square coefficient, the A_3*V_{PTAT} can be decomposed as follows.

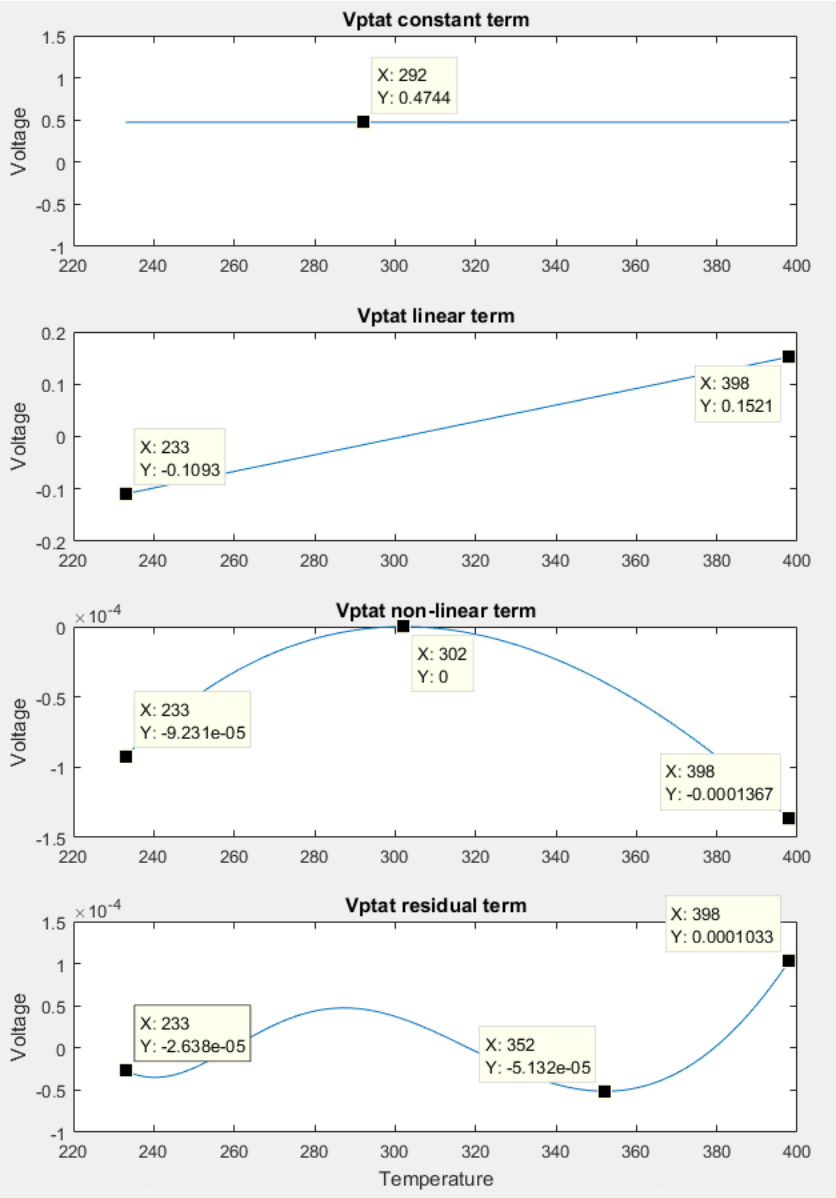


Figure 26 : Decomposition of V_{PTAT} component

After multiplication with the least square coefficient, the A_3*V_{PTAT} has a 474mV constant term with a peak-to-peak variation of 261mV for the linear term, 136uV for the non-

linear term and 154uV residual term. It is noted that there is a decent non-linearity in the V_{PTAT} term as well, that needs to be compensated for, along with the non-linear voltage term.

A_2*V_{NL} can be decomposed as follows.

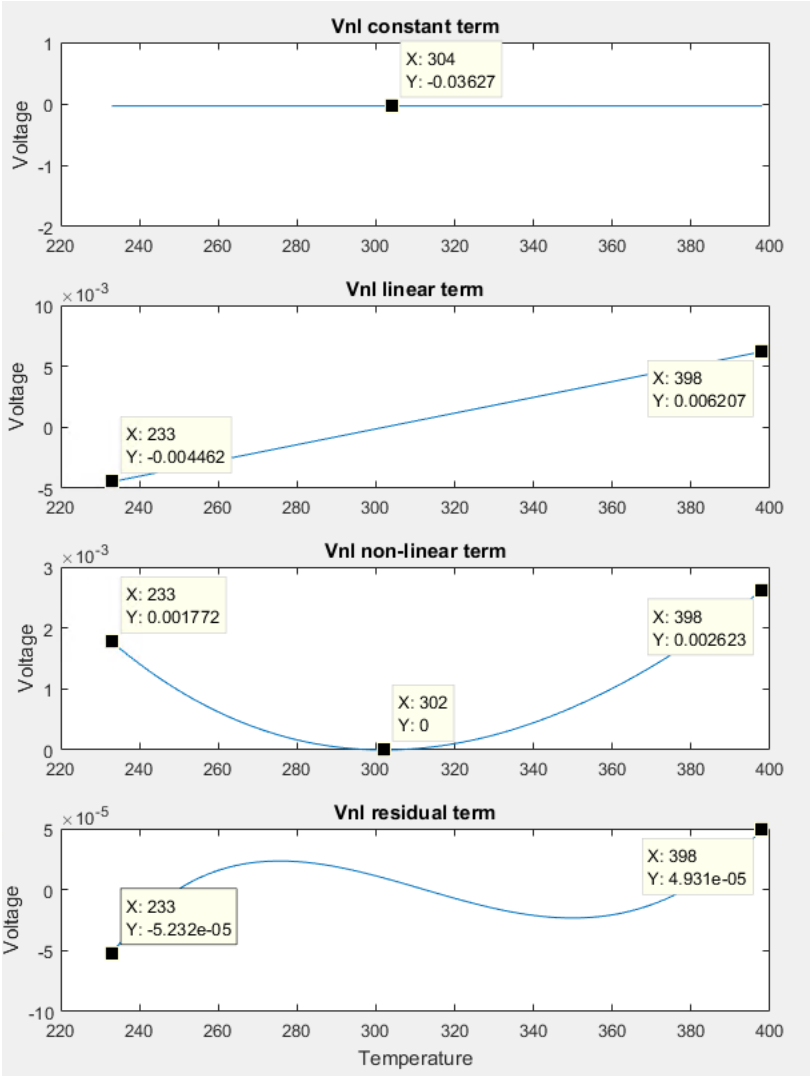


Figure 27 : Decomposition of A_3*V_{NL}

A_3*V_{NL} has a -36mV constant term with a peak-to-peak variation of 10.6mV for the linear term, 2.6mV for the non-linear term and 101uV residual term.

From the non-linear components of the V_{NL} and V_{BE} terms, it can be inferred that they compensate each other, leaving behind a 191uVpp (peak-to-peak voltage, contributing to

1ppm/°C approximately) which gets added to the 154uVpp corresponding to the non-linearity in the PTAT voltage.

The coefficient of V_{BE} is set to unity based on the analysis done in (43)-(45), since the term V_{GO} is present in the V_{BE} expansion. But, from Figure 25, constant component of V_{BE} is much smaller than the value of V_{GOr} (1.1478 V). Setting the coefficient A_1 to unity adds a limitation to the choice of coefficient A_2 and A_3, which results in the constant term being set to the desired value, but the temperature dependent components are not equally well-compensated. This result may be expected, considering the voltage variations present in the component terms that are targeted to be compensated using constant coefficients.

The use of the extrapolated value of bandgap voltage, V_{GOr} for the fitting procedure presents another error that is introduced in the analysis and may be unsuitable. Hence, another approach for determining the coefficient utilizing only known coefficients to determine the unknowns needs to be adopted.

5.6.3 Proposed Method of V_{GO} Extraction Using Least Square

The analysis needs to be independent of any uncertainties or unknown quantities, as to extract the bandgap voltage accurately. The fitting approach should be performed such that all the known quantities are utilized to determine the unknown coefficients. Based on mathematical analysis from (43)-(45), it has already been established that the coefficient of V_{BE} is unity. Hence the known quantities in (41), A_1*V_{BE} along with the measured voltages, V_{PTAT} and V_{NL}, are used to determine the unknown quantities-A_2, A_3 and the output reference voltage (bandgap voltage).

$$V_{BE} - e(T) = V_{REF} + (A_2')V_{NL} + (A_3')V_{PTAT} \quad (47)$$

where A_2' (= -A_2) and A_3'(= -A_3) are the new coefficients; e(T) represents the errors associated with the system such as measurement noise, which is small and neglected in the analysis.

$$[V_{BE} - e(T)] = \begin{bmatrix} 1 & V_{NL}(T_1) & V_{PTAT}(T_1) \\ 1 & V_{NL}(T_2) & V_{PTAT}(T_2) \\ . & . & . \\ . & . & . \\ 1 & V_{NL}(T_{166}) & V_{PTAT}(T_{166}) \end{bmatrix} \begin{bmatrix} V_{REF} \\ (A_2') \\ \\ (A_3') \end{bmatrix}$$

Once the unknowns are determined, V_{REF} is obtained as follows.

$$V_{REF} = V_{BE} + (A_2)V_{NL} + (A_3)V_{PTAT} \quad (48)$$

The technique was used to determine the coefficients as

A_2 = -3.3325

A_3 = 6.1431

The value of V_{REF} obtained from the least square analysis is 1.1234V. Substituting the coefficients in (48) generates a V_{REF} having a temperature coefficient of 0.2674 ppm/°C with a peak-to-peak variation of 49uV.

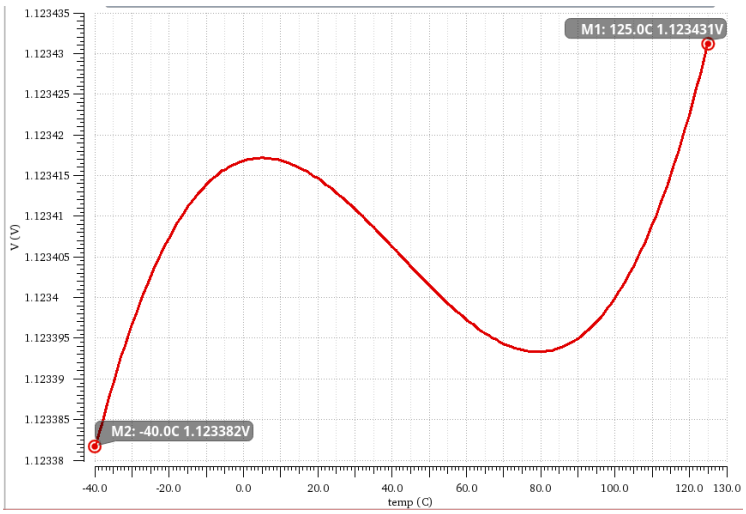


Figure 28:Output obtained after linear recombination

It is observed that the output has a visible PTAT profile and can be made symmetric by slightly tuning the V_{PTAT} coefficient. For a more accurate value, the fitting procedure needs to utilize the infinity norm. Least square fitting utilizes L2 norm, which is simpler and easier to implement. Modifying A_3 to 6.1425 results in an output V_{REF} having a temperature coefficient of 0.1772 ppm/°C with a peak-to-peak voltage variation of 33uV.

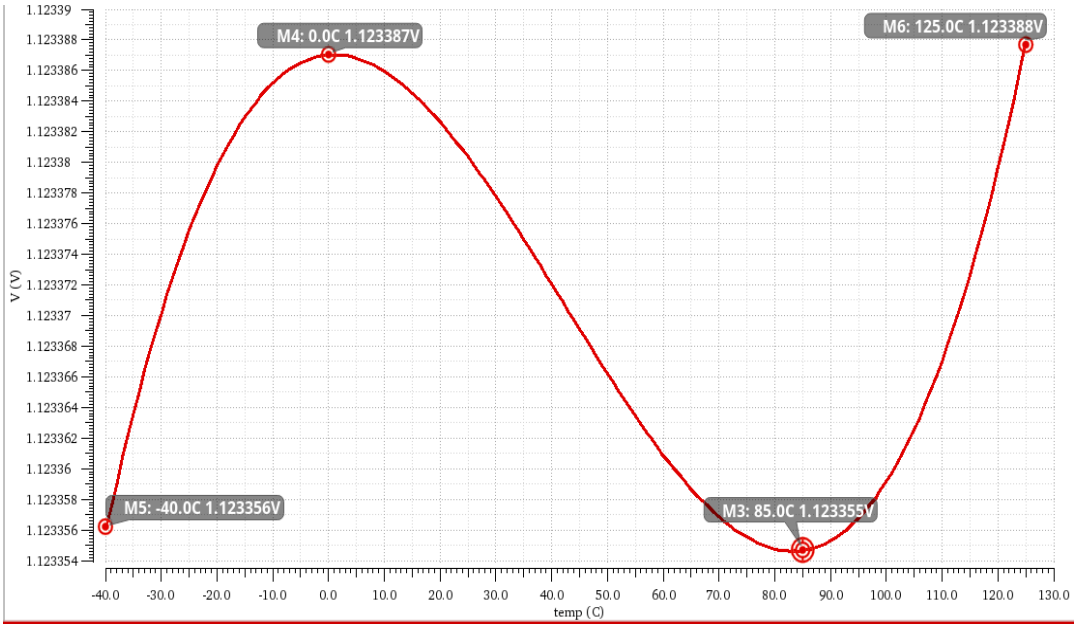


Figure 29:Output profile after tuning A_3

5.7 Implementation of V_{GO} Extraction

As explained earlier, various techniques may be used for implementing (48). The implementation can even be performed in the voltage or current domain. This thesis will focus on the analog voltage domain implementation as shown in Figure 30**.**

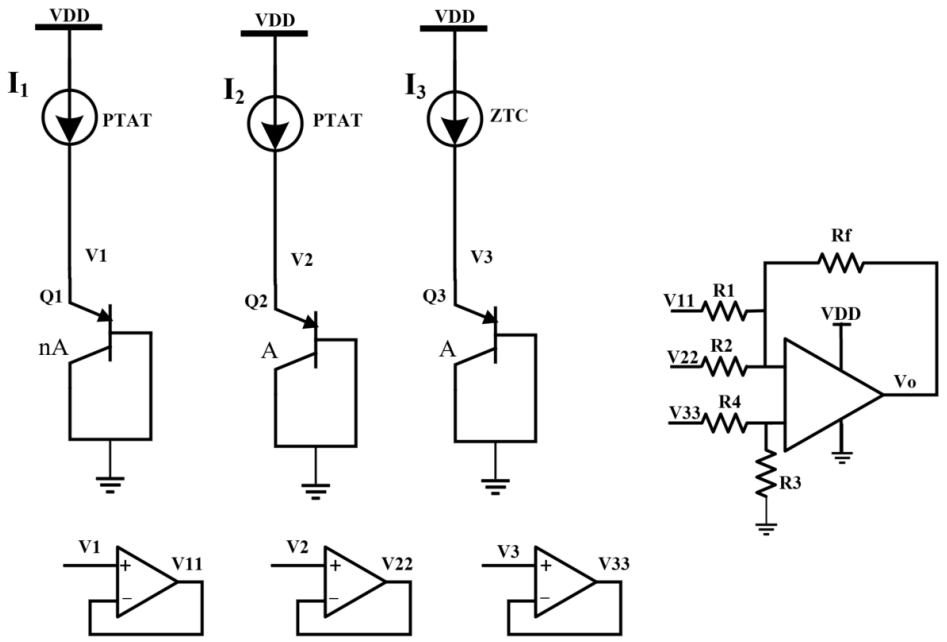


Figure 30: Conceptual illustration of the extraction concept

It is essential that buffers need to be placed before the required linear combination, in order to prevent the biasing currents from flowing through the gain stages and affecting the base-emitter voltage values. The gain/coefficients can be implemented using existing resistor values.

The voltages V_{PTAT} and V_{NL} are essentially arithmetic voltage variants of the base emitter voltages across the transistors. Hence, instead of dedicating circuit structures designed to explicitly generate the difference terms, (41) can be rearranged as shown.

$$V_{ref} = A_1V_2 + A_2(V_3 - V_2) + A_3(V_2 - V_1)$$

$$V_{ref} = (-A_3)V_1 + (A_1 - A_2 + A_3)V_2 + (A_2)V_3$$

$$V_{ref} = (B_1)V_1 + (B_2)V_2 + (B_3)V_3 \quad (49)$$

This was simulated in Cadence using existing resistor values to implement the gain as shown in Figure 31.

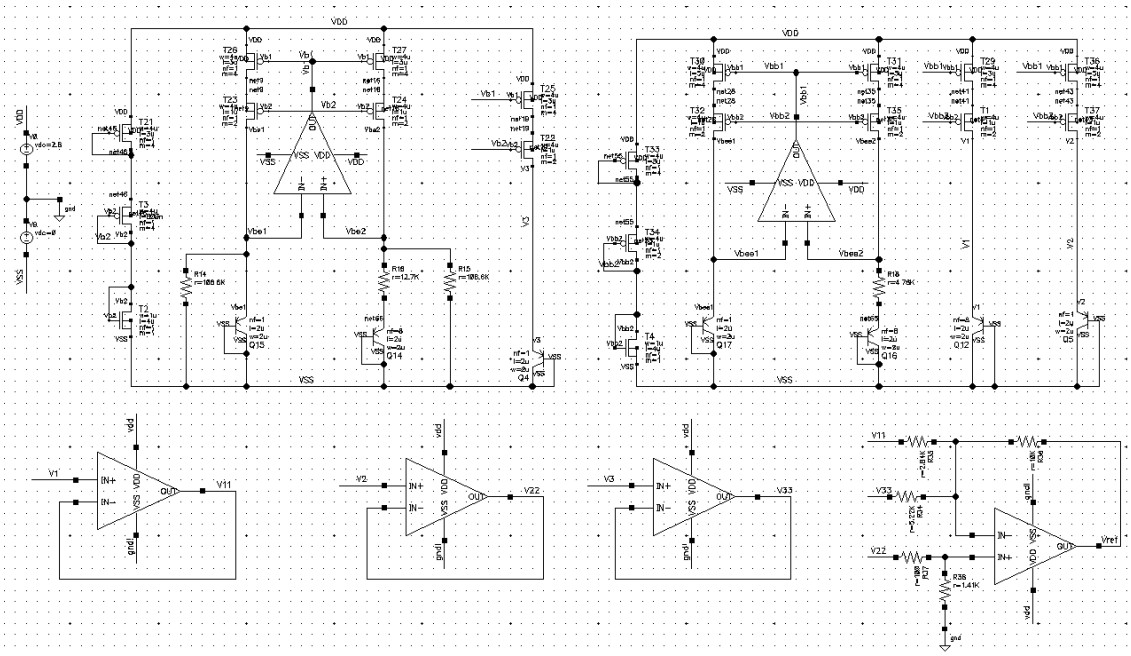


Figure 31: Schematic of the implementation in Cadence

The output reference voltage is shown in Figure 32 and the temperature coefficient is 0.3226ppm/°C, with a peak-to-peak output voltage variation of 34uV. It is to be observed that output voltage is not 1.14V, which is the bandgap voltage, but a fraction of V_{GO}. This is for the ease of implementation using the existing resistor values as described in the following section. The spice model of ADA4528 was used for implementing (49).

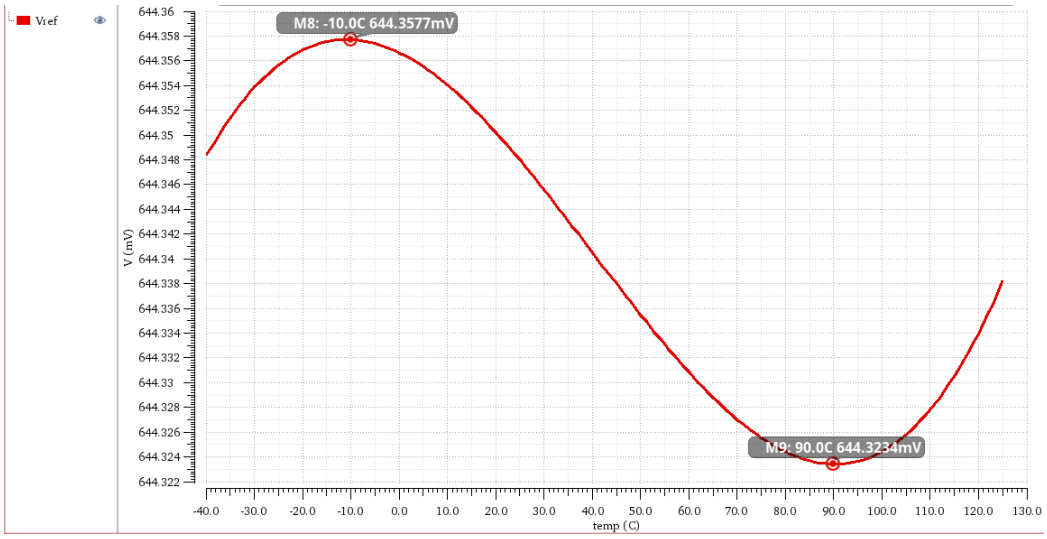


Figure 32:Output after implementation in the analog domain

5.8 Challenges in the Implementation

Since constant coefficients are used to compensate and cancel out the high voltage variation in the V_{PTAT}, V_{NL} and V_{BE}, it is expected that the output voltage reference and its temperature coefficient will be highly sensitive to the coefficients. It is desired to accurately implement (49) using a suitable summing/difference amplifier configuration. The temperature coefficient and tolerance of the resistors are not considered during the simulation. If all the resistors have the same temperature coefficient, then it is likely that they cancel each other since the summing structure utilizes resistor ratio for implementing the gain. There are new processes that have zero temperature coefficient resistors and trimming techniques may be adopted to realize the resistor values accurately.

The spice model of the op amp used has a systematic offset, but random offset/temperature effects are not modeled. Hence the simulation does not take the op-amp drift into account and this introduces error in the analysis.

In section 5.6.2 and 5.6.3, a 166-point fitting approach is adopted. In the implementation of the proposed concept, measuring the base-emitter voltages at 1°C steps across the desired temperature range, are time consuming, expensive and not practical. Hence, a modified approach is put forth, in Section 5.9.

5.9 Modified Least Square Fitting to Determine the Coefficients

Now the task is to determine if similar performance may be achieved using voltages recorded across fewer temperature values. The results of a nine-point fitting and a four-point fitting approach are explained below and the corresponding temperature coefficients of the outputs are compared with that using 166-point fitting.

5.9.1 Nine-Point Fitting for Coefficient Generation

The approach described in Section 5.6.3 is experimented using the voltages taken at 9 temperatures and the coefficients A_1, A_2 and A_3 are estimated. The temperatures were so chosen to trace the third-order profile curve (Two temperatures at each rising and falling edges and the peaks of the curve). The base-emitter voltages were recorded at -40°C, -20°C, 0°C, 40°C, 60°C, 85°C, 105°C, 115°C and 125°C and the coefficients were obtained as follows:

A_2 = -3.3290

A_3 = 6.1443

V_{REF} obtained using least square analysis is 1.1235V.

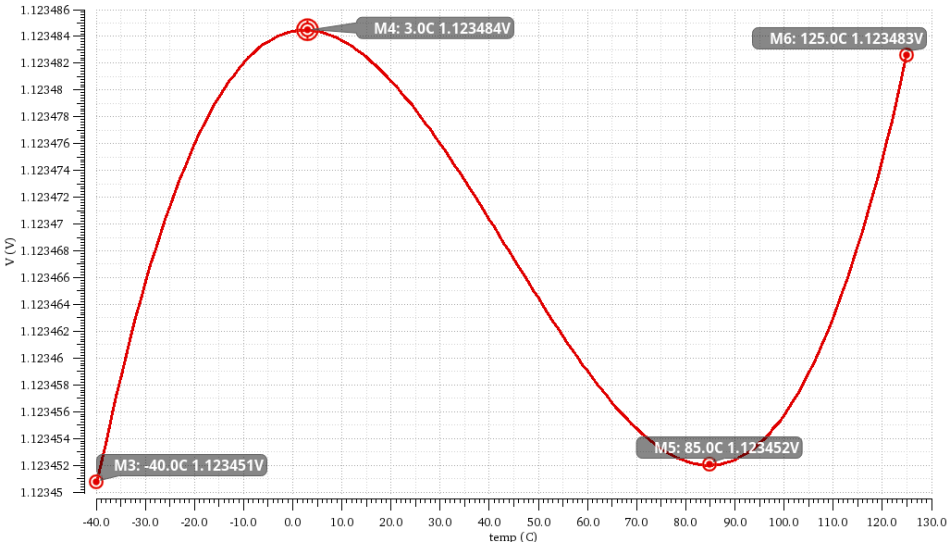


Figure 33:Output obtained using 9-point fitting

The output, when implemented using ideal components, has a temperature coefficient of 0.18ppm/°C, which is in the targeted sub-ppm/°C range.

5.9.2 Four-Point Fitting for Coefficient Generation

Since, the targeted performance was achieved using 9-point fitting, an approach was taken to reduce further the number of points taken for the analysis. Now, the analysis was repeated using the base-emitter voltages recorded at -40°C, 0°C, 85°C and 125°C (extreme temperatures and peaks) and the coefficients were determined as:

$A_2 = -3.3325$

$A_3 = 6.1431$

V_{REF} obtained using least square fitting equals 1.1234V.

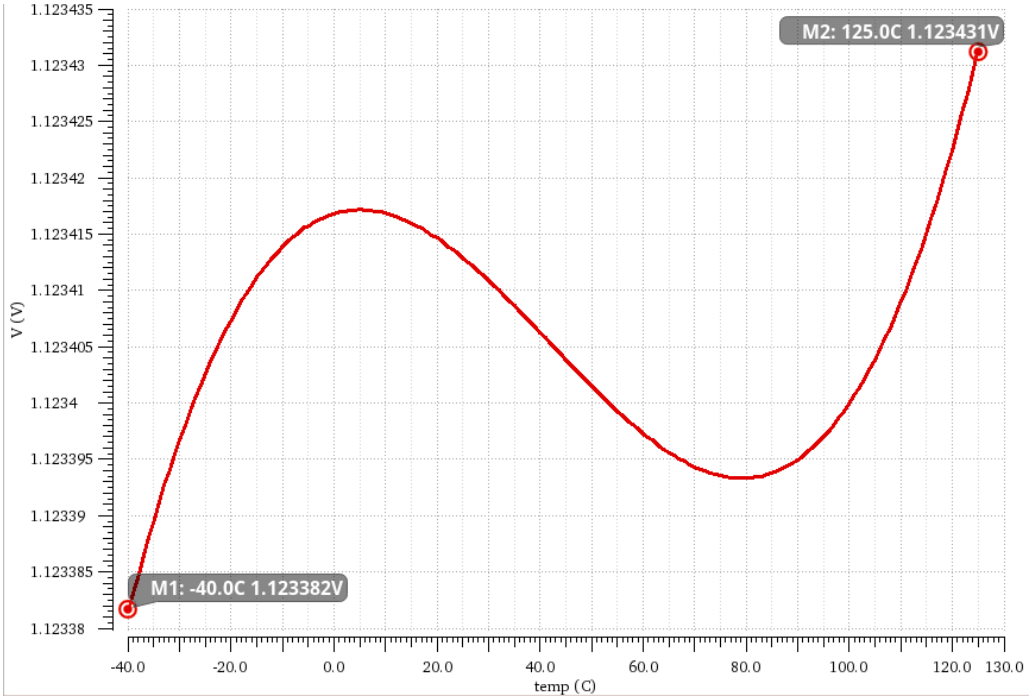


Figure 34 : Output obtained using 4-point fitting technique

The output obtained after linear combinations using the calculated coefficients had a temperature coefficient of 0.267ppm/°C, which is within the targeted sub-ppm range. The profile of output can be made more symmetric by slightly modifying the coefficient.

CHAPTER 6: MEASUREMENT RESULTS

The section describes the design and implementation of the extraction technique in a Printed circuit Board (PCB) and the associated measurement results. The test-set up is briefly discussed, and the observations are presented. The three key diodes were fabricated in UMC-65nm process. The IC layout with the diodes and the bonding diagram is shown in Figure 35. The diodes are laid out in a common-centroid fashion for better matching, in the ratio 2:2:12. The die was packaged using a 24-pin Dual-In-Line ceramic package**.** Ceramic packages are known to induce low package-shift.

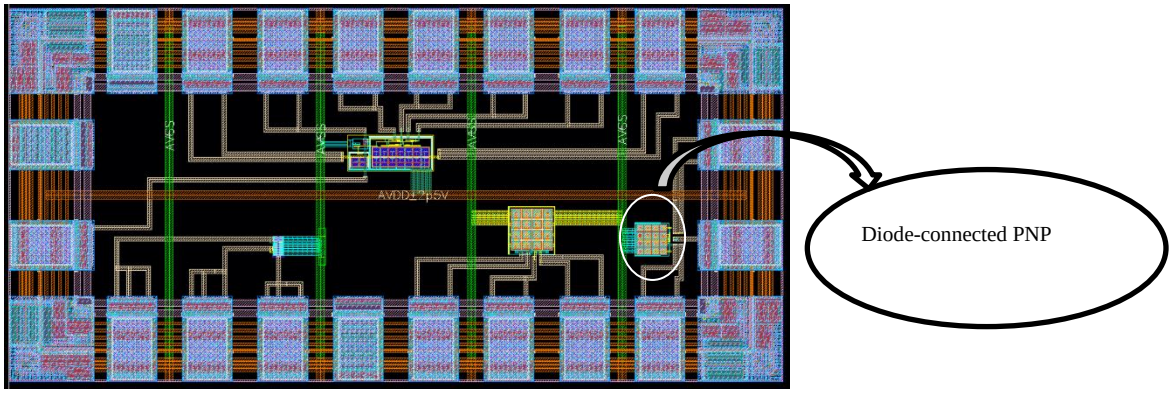


Figure 35: On-chip diodes

6.1 Choosing the Components

This section explains the various aspects considered while choosing the components required for the V_{GO} extraction. The details regarding the measurement set-up and equipment description are presented in 6.3.

The task is to implement the circuit in Figure 30. Since the diodes are the only components present on-chip in the implementation, the set up requires external current sources, buffers and the summing amplifier. The measurement procedure involves biasing the diodes with appropriate PTAT and ZTC currents, measuring the base-emitter voltages across the diodes across a range of temperatures and post-processing the data to determine

the coefficients using the least-square fitting approach described in 5.6.3. This procedure is used to choose the resistor values for the summing amplifier and subsequently measure the output of the summing amplifier.

The validation of the circuit involves accurate temperature control and measurement. For the analysis, the temperature may be maintained using a thermal bath or oven. Since an on-chip current source is not used, external means to bias the diodes are required. One approach involves the use of source measure unit/SMU for programming the current sources to mimic a PTAT profile (I_1, I_2) and a ZTC current (I_3). The SMU is programmed to input a specified current at a given temperature. Another possible approach involves the use of a commercially available current source for sourcing the bias currents I_1 and I_2 in Figure 30 and SMU for sourcing current I_3. LM 134 is used to provide the bias currents I_1 and I_2. This is a commercially available three-terminal, adjustable current source that supports operation across the desired range of temperatures (-40°C to 125°C) and sources a current that is PTAT in nature. The system was designed such that $I_1 = I_2$ and $V_{BE2} = V_{BE3}$ at the reference room temperature. Since the equations (35)- (45) utilizes the base-emitter voltages across the diodes alone for coefficient determination, the first set of measurements (recording the base-emitter voltages, before post processing) is done in the absence of the active circuitry (buffers and summing circuit) to avoid any errors in the extraction procedure.

An op-amp IC is required for operating as a buffer and a summing amplifier. The offset-voltage, offset-voltage drift and bias current may act as potential sources of errors in the system. An op-amp with higher offset-voltage and associated drift may result in shifts in the voltages V_1, V_2, V_3 across the desired temperature range, which in turn affects the recombination. The bias current of the op-amp may result in error voltages, which affect the

performance. ADA4528 is a precision, zero-drift op-amp with ultralow offset voltage, across -40°C to 125°C. The bias current is in the order of hundreds of pico-amperes across temperature. The op-amp was configured in a single-supply operation at 2.5V.

The resistor values in the summing stage were determined by the coefficients A_1, A_2 and A_3. Resistors having a temperature coefficient of 25ppm/°C were chosen for the implementation.

6.2 PCB Design

A two-layer printed circuit board was designed for testing the V_{GO} extraction concept. For measuring and debugging purposes, provisions were made for the measurement of V_1, V_2, V_3 (the base-emitter voltages across the three diode-connected transistors), V_{11}, V_{22}, V_{33} (the output of the buffer) shown in Figure 30 and V_{OUT} (the output of the summing amplifier). Standard banana plugs were used to provide connections from the board to the measurement instruments.

COMPONENT	FUNCTION
LM134	Current source
ADA4528-2	Buffer and Summing Stage
0.1µF Capacitor	Decoupling capacitors
10kΩ resistor(25ppm/°C)	Summing Stage
5kΩ resistor(25ppm/°C)	Summing Stage
1.38kΩ resistor(25ppm/°C)	Summing Stage
1.45kΩ resistor(25ppm/°C)	Summing Stage
1.78kΩ resistor(25ppm/°C)	Summing Stage
10Ω resistor(25ppm/°C)	Summing Stage
10Ω resistor(25ppm/°C)	Summing Stage

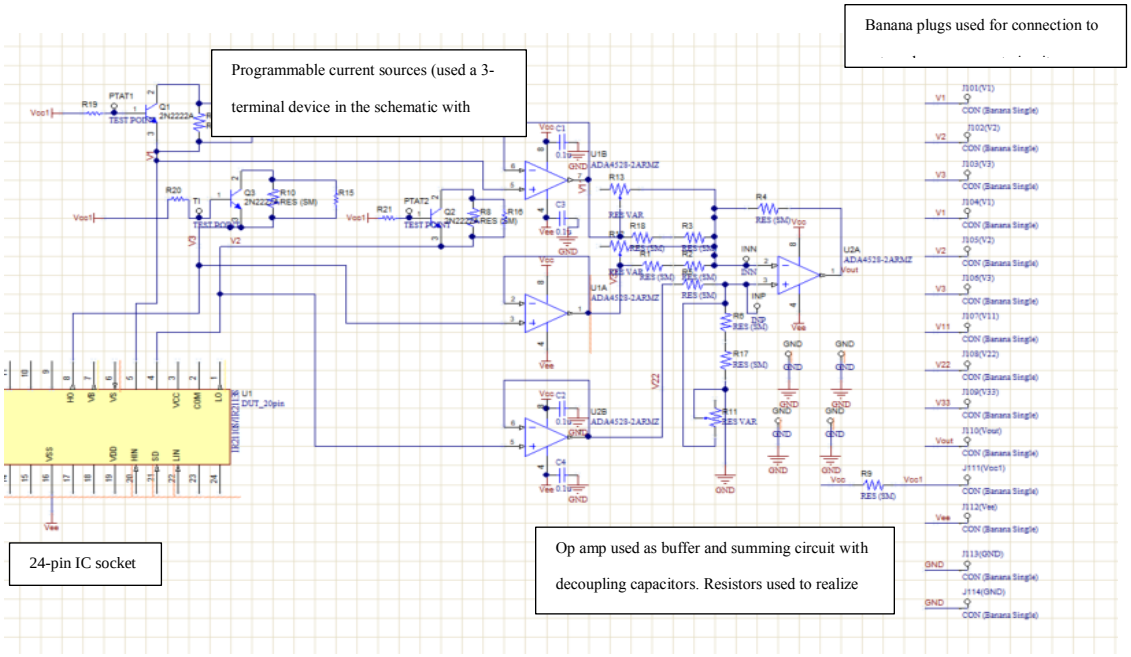
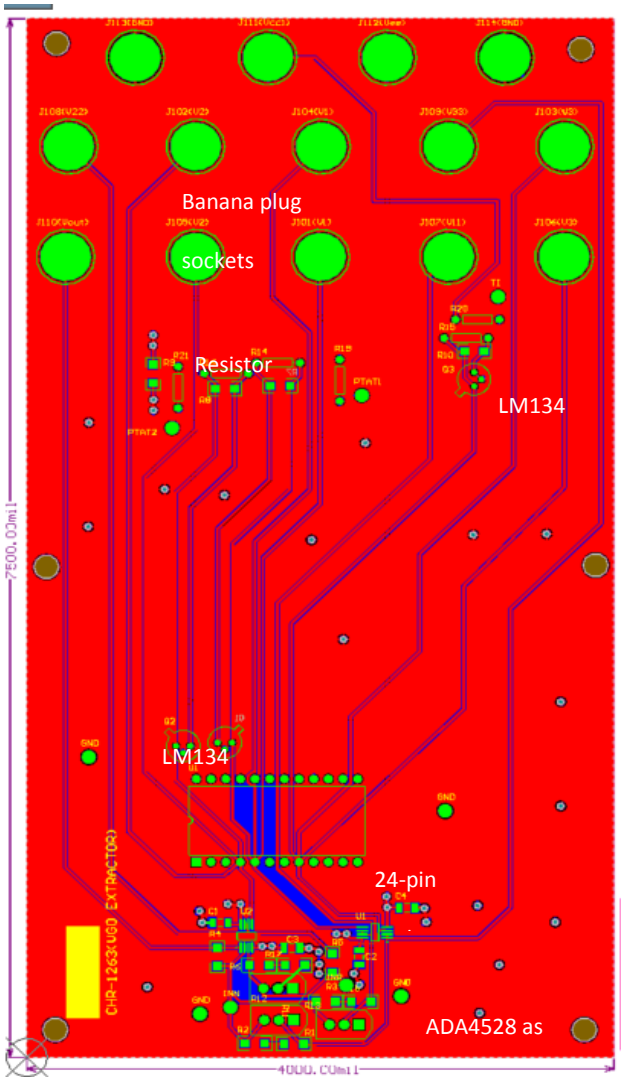


Figure 36: PCB schematic

Special care was taken to minimize the PCB effects on the performance of the circuit. The significant PCB effects that can affect the system include the errors caused by board leakage, trace resistances, improper grounding etc. Even nano-amperes of leakage currents can generate hundreds of micro-volt error in the measured output, which lowers the temperature coefficient by a few ppm/°C. Similarly, without the use of 4-point Kelvin connections, the voltage drops across the trace-resistances will be included in the measurement of the base-emitter voltages. Errors in the base-emitter voltages may affect the post-processing and the appropriate coefficients may not be generated.

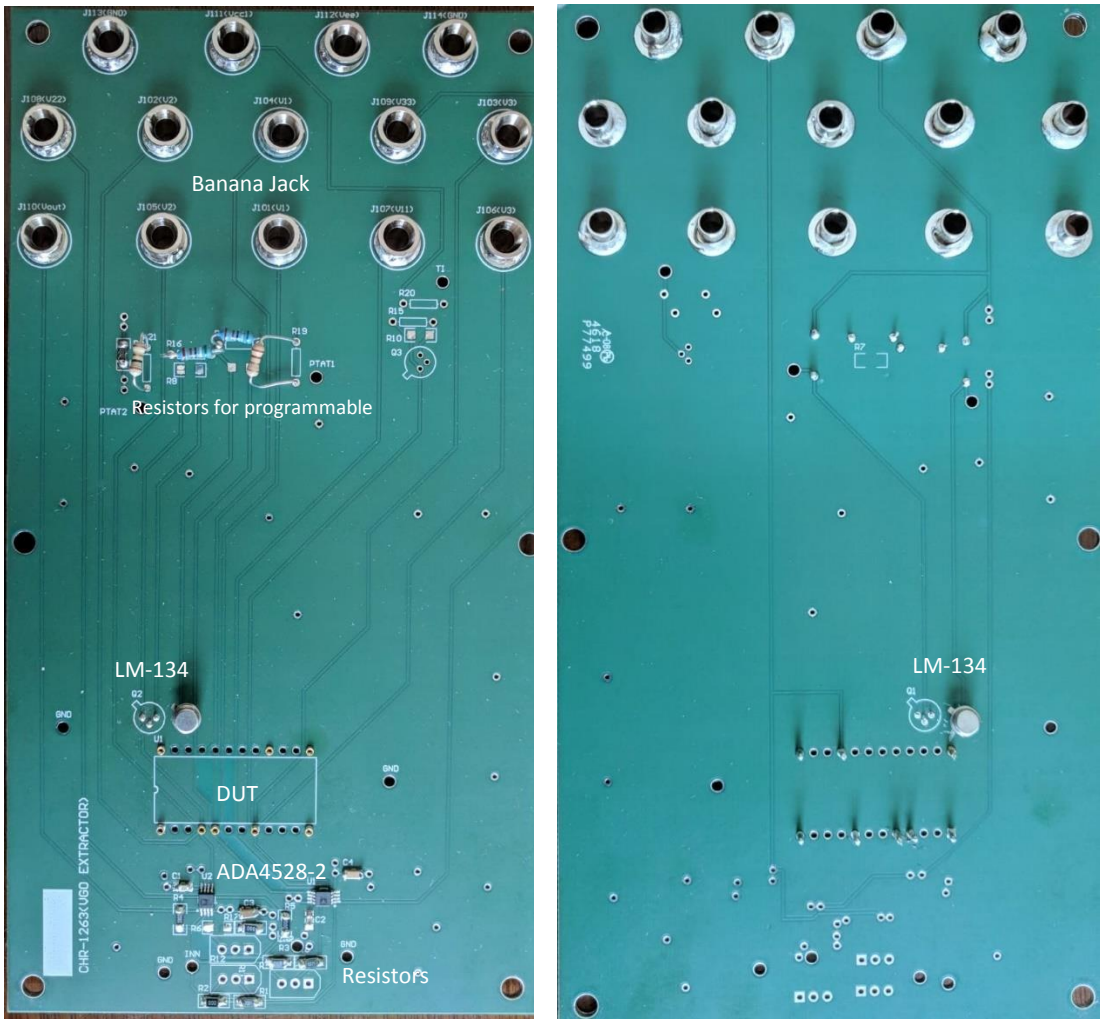
FR-4 material was used to make the board rigid and less prone to any stress, as to minimize the error due to leakage currents. The PCB may be contaminated after soldering, by residual flux or other salts, which can create leakage paths-hence, it was ensured that the board was thoroughly cleaned using deionized water in an ultrasonic bath and baked at 85°C for 15 minutes, following each soldering/de-soldering. The measurements were done using a 4-point or Kelvin connection. Separate force and sense paths were provided for the

measurement of the base-emitter voltages across the diode. The multiple measurement points added for debugging, along with the force and sense wires, resulted in many signal traces on both the top and bottom layer of the board. Consequently, it was difficult to dedicate an entire layer as a ground plane. Polygon/copper pours that were connected to the ground using stitching vias, were created. Power supply pins were decoupled to the ground using decoupling capacitors.



(37.1)

Figure 37: (37.1) PCB Layout (37.2) Fabricated PCB with soldered components (2 sides)



(37.2)

To prevent any thermal error due to Seebeck effect and ensure that all the components were maintained at the same temperature, the entire circuit was laid out in the bottom section of the board, with traces coming out to the top section and terminating at a banana jack, for connection to the measuring instruments. This is because the temperature is inconsistent in the bath which is explained further in 6.3. Furthermore, the banana plugs cannot be exposed to high temperatures and cannot be immersed in the bath.

A 24-pin socket was soldered to the board to hold the chip (DUT). The op-amp, decoupling capacitors and resistors were surface-mount components. Discrete resistors were

used to implement the coefficients in (49). Due to the high sensitivity to the resistor values, it is desired to use resistors with low temperature coefficient and tolerance. All standard values of such highly accurate resistors are not available. They are manufactured to-order and have a lead time of at-least 90 days. If standard resistors are not readily available to implement the coefficients, the capability to use resistors in series (the closest standard resistor value and a small resistor value) to provide some degree of tuning was added in the printed circuit board. If series resistors are not required, then one of the resistors is replaced by a zero-ohm resistor to ensure connectivity. A capability to utilize tuning/variable resistors in place of discrete resistors was also designed in the board. However, the commercially available variable resistors have a high temperature coefficient and there would be a higher mismatch between the resistors, which can cause errors. Provisions were made to accommodate both surface-mount and through-hole resistors.

6.3 Measurement Setup

This section details the measurement procedure and the description of the instruments used. The test procedure involves utilizing the bath to maintain the circuit at the desired temperature, forcing the currents through the three diodes and recording the base-emitter voltages across the desired range of temperatures. This process involves synchronization between the instruments for achieving the desired level of accuracy. If the temperature is not accurately maintained, it will affect the coefficient-generation. The bath, the current sources and the digital multimeters used for measurement are programmed using TestStand, which is a software developed by National Instruments for automated tests.

The section of the board with the circuitry is immersed in a thermal bath. An oven may also be used for temperature-based measurements, but the temperature can be accurately controlled only up to ±3°C. Julabo refrigerated heating circulator (Model number: FN32-

HE), with a working temperature range from -35°C to +200°C was used for maintaining the temperature in the system. The system offers temperature stability of ±0.02°C. The bath fluid, Thermal H10, used in the circulator has a working temperature range from -35°C to +180°C. Operating outside the specified temperature range would damage the circulator. All the measurements were done in the temperature range from -35°C to +125°C. It is to be ensured that the bath fluid in the circulator always remains above a certain threshold limit.

Another aspect for consideration is the uniformity of the temperature inside the bath. There exists a temperature gradient inside the bath. The temperature is most accurately maintained at the bottom of the circulator and gradually decreases upwards. Hence the entire circuit is laid out at the bottom section of the board to provide accurate temperature control.

Keysight Technologies B2912A Precision Source/Measure Unit, a dual channel instrument is used for sourcing currents I_1 and I_2, which is PTAT in nature. Keithley 2400 Source Measure Unit is used for sourcing the ZTC current I_3. The PTAT profile current values, in amperes and the temperature, in Celsius (used in simulation) recorded at 1°C interval is exported into the software. The SMU is programmed such that when the bath temperature is set to the desired temperature, SMU sources the programmed current value corresponding to the set temperature.

An alternative arrangement used for forcing the desired currents I_1 and I_2 is the use of the current source LM-134, which is soldered on to the board. The current source is also immersed in the bath for generating a current, that is PTAT in nature. I_3 is generated using the SMU. The SMU is programmed to source I_3=11.3uA, that mimics the ZTC current in simulation, having a temperature coefficient of 12.4ppm/°C.

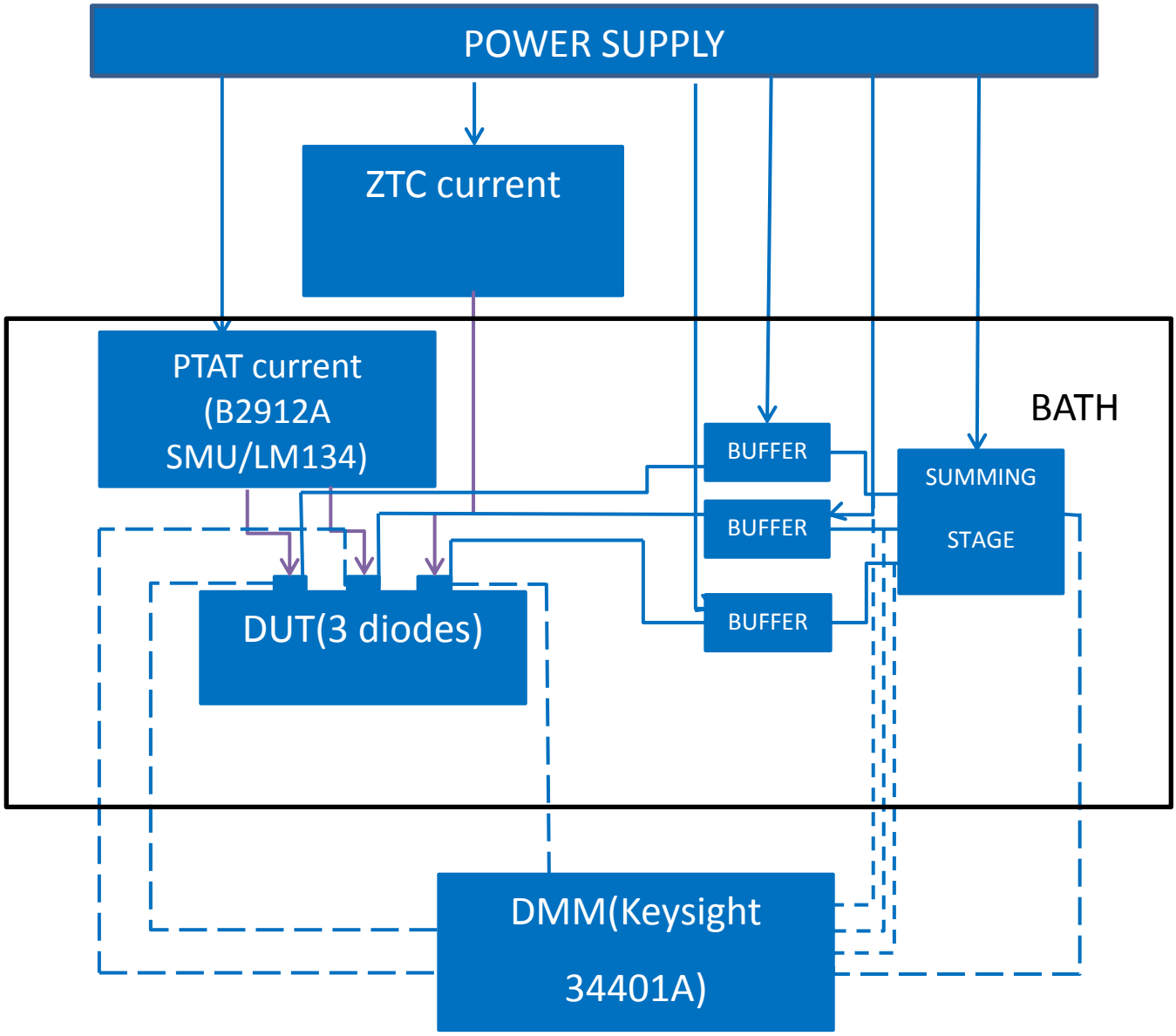
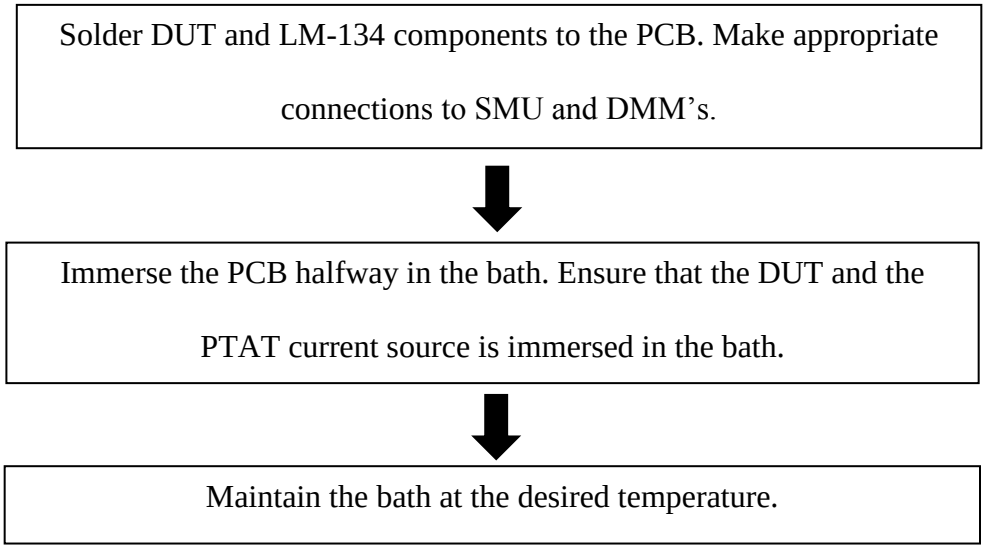


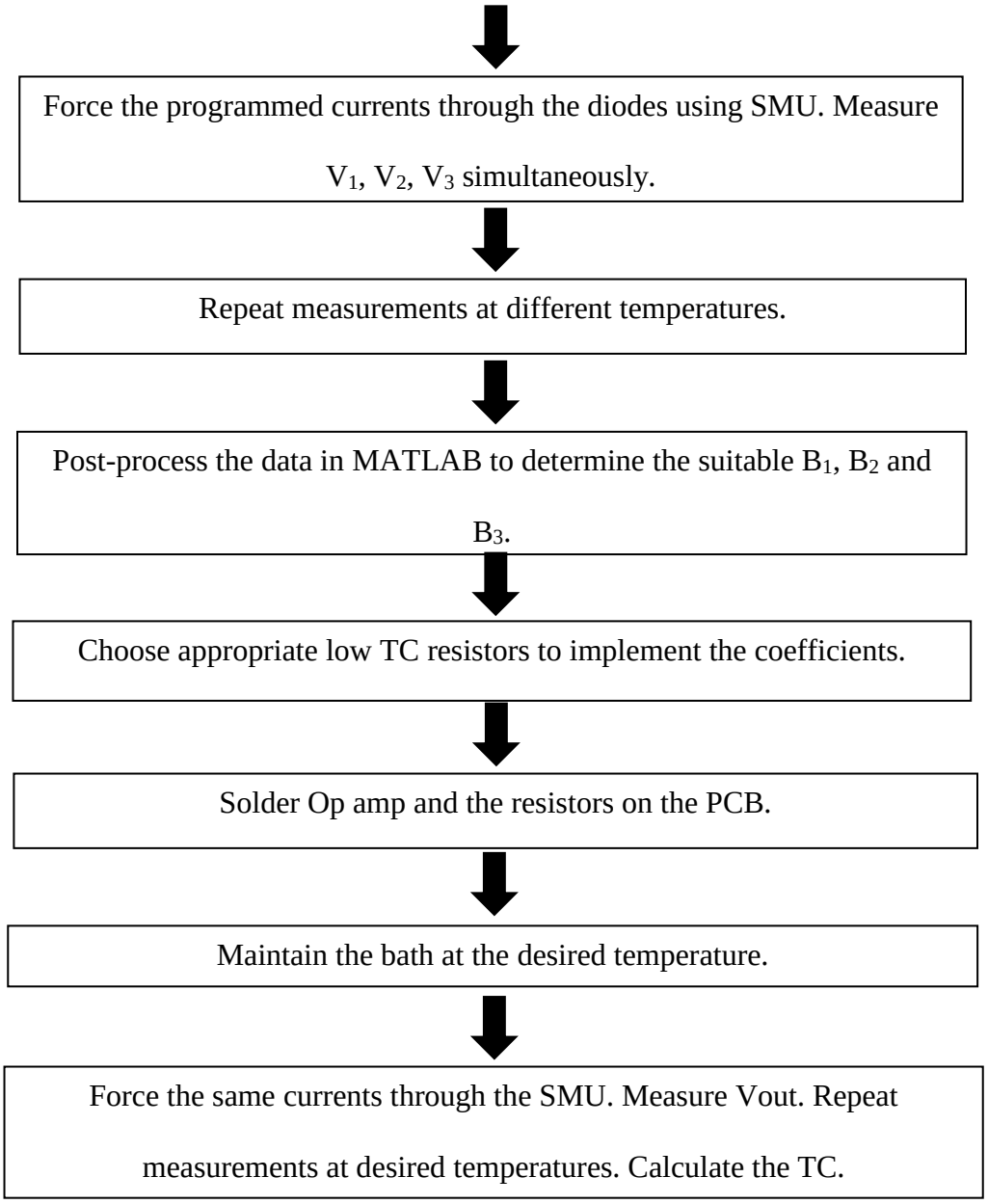
Figure 38: Block diagram depicting the measurement setup

Across the temperature range from -35°C to 125°C, every 160uV contributes to 1ppm/°C temperature coefficient, hence the measurement device should be capable of accurately measuring the voltages at least in the order of hundreds of microvolts. The source measure units mentioned above can source the currents with the desired accuracy but cannot provide the desired measurement accuracy. Keysight Technologies 34401A digital multimeter offers measurement accuracy within tens of microvolts and hence is more suitable for the required measurement. Once the Source Measure Units source the programmed

currents across the diodes, the Multimeters record the desired voltages and the data is stored in the computer. The DMM's are programmed such that the voltages are recorded simultaneously across the three diodes to avoid any time-drift error.

TestStand allows to automate the tests, by introducing a loop in the program to perform the following procedures for the desired temperatures ranging from -35°C to 125°C. The thermal bath is in the set in the Soak mode so that the temperature gradually settles to ±0.02°C within the desired temperature and then it is in the Set mode. The SMU's are turned ON and each SMU sources the programmed current corresponding to the set temperature. The DMM's are then turned ON one by one and after a 1-second delay, all the required voltages are recorded and stored in the computer. Then the DMM's are turned OFF and the system goes to the next iteration in the loop (the soak mode to set the next chosen temperature). Once the temperature reaches 125°C, the thermal bath is programmed to set the temperature back to 25°C and all the measurement instruments are turned OFF. This is because the bath fluid evaporates fast at higher temperatures and if left unnoticed, it may go below the warning limit. A flowchart detailing the measurement procedure is presented below.



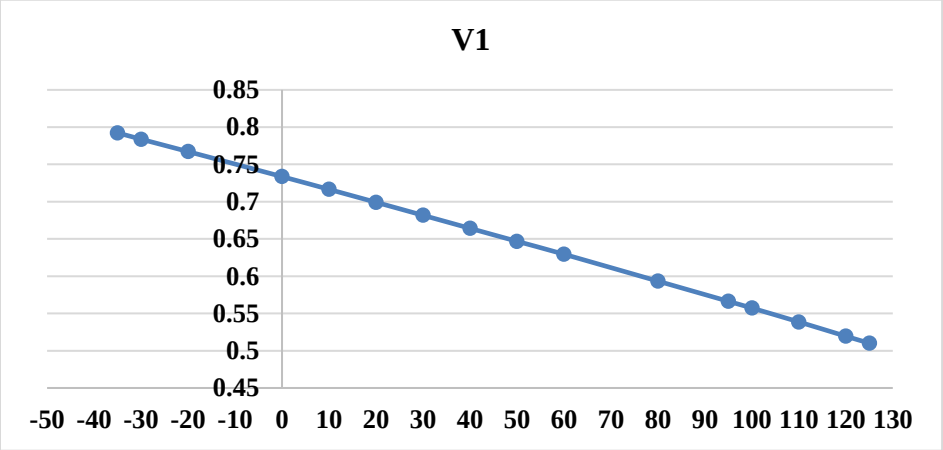


6.4 Measurement Results

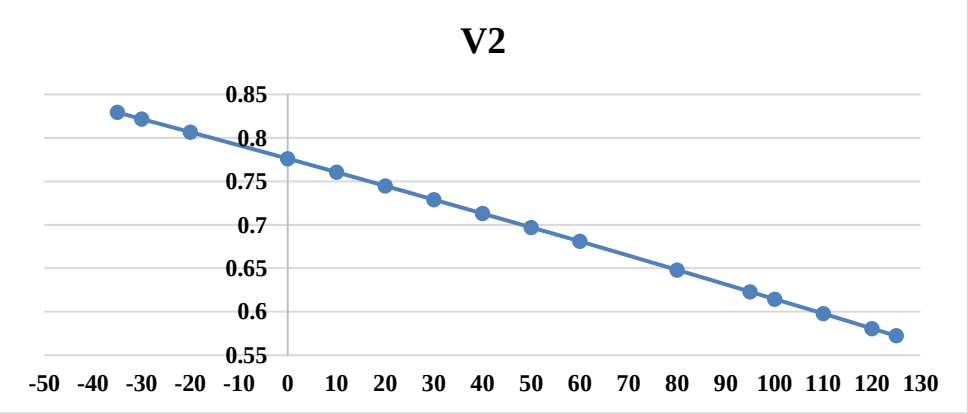
This section presents the measurement results and observations. The PTAT generator LM-134 sources current in the range 8µA-15µA across the desired temperature range. The ZTC current source is programmed to source an 11.3uA current, similar to the simulation set up.

The initial set up results indicated the measurement results being affected by noise in the system. To average out the measurement noise, the system was programmed to record 31 readings at a given temperature, and the averaged voltage value was used for the analysis. All the measurement results shown below correspond to the voltage values obtained after averaging at each temperature.

The measured base-emitter voltages across the diode-connected transistors Q_1, Q_2 and Q_3, were plotted across the temperature range -35°C to 125C as shown in Figure 39. The measurements were done in the absence of any additional circuitry as in Figure 14.

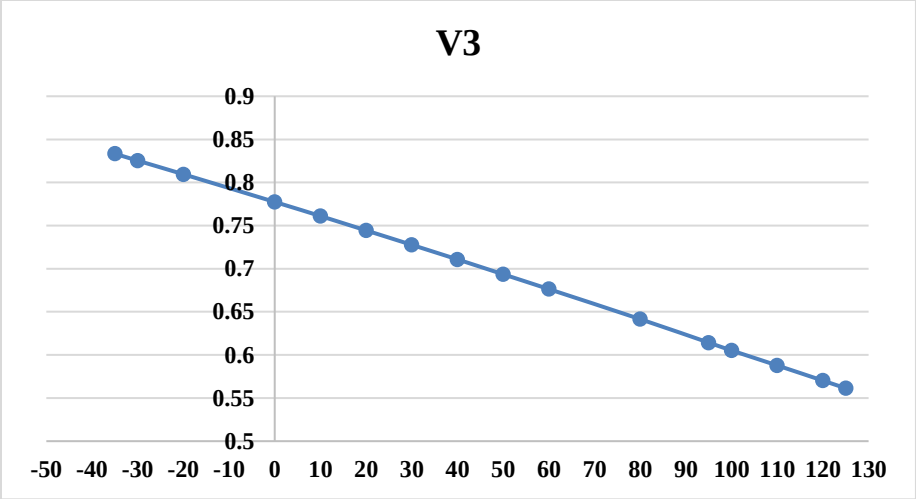


(39.1)



(39.2)

Figure 39:Measured Diode Voltages



(39.3)

Figure 39 (continued)

Across a few temperatures from -35°C to 125°C, a few voltage readings among the 31 measured voltage readings corresponding to V_1 recorded a spread in the voltage instead of being clustered together to average out to specific value. Repeating the measurements across the same temperature range immediately following the first run fixed the issue. The result may be an error introduced due to cold solder joints. The reheated joints seem to have reduced the problem, but a few runs still displayed voltages at random temperatures, that did not follow the trend and they were eliminated from the post processing.

While performing the least square analysis, the measured values were rounded to 4/5 digits before fitting tom minimize the effect of measurement noise. It was observed that the fitting procedure was more accurate when fewer measured voltages were utilized. This may be mostly, because of external noise and hence the 166-point fitting approach and 9-point fitting approach were not the most suitable since it is hard to track down which temperature causes the issue. The four-point fitting approach seems appropriate, considering this aspect.

The voltages recorded at -30°C, 0°C, 80°C and 125°C were utilized for determining the coefficients. The coefficients were determined as follows:

$B_1 = -7.2464$

$B_2 = 13.2464$

$B_3 = -5$

The resistors were chosen to implement the coefficients in (49). The resistors R_3 and R_4 were not used and the voltage V_{22} was directly connected to the positive terminal of the op amp.

$R_f = 10k\Omega$

$R_1 = 1.38k\Omega$

$R_2 = 2k\Omega$

Due to lack of availability of low temperature coefficient standard resistors, resistors having a temperature coefficient of 25ppm/°C were used in the implementation. The additional circuitry was appended, and the board was thoroughly cleaned in an ultrasonic bath before testing. The output/reference voltage recorded at Vout is shown in Figure 40.

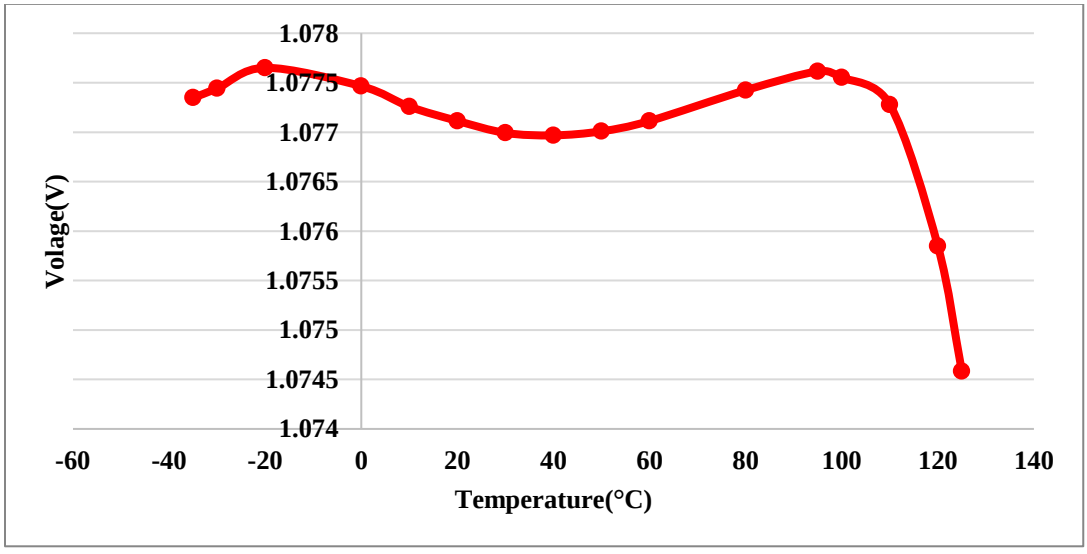


Figure 40:Measured V_{OUT}

The resultant temperature coefficient of the measured output is 18ppm/°C across the temperature range of -35°C to 125°C and is attributed to the 2mV tail observed after 100°C, which is not expected. If the temperature range is restricted to 85°C, the output has a temperature coefficient of 4.57ppm/°C, which may be reasonable considering the minimalistic set up used for validating the approach. To debug the source of this voltage-drop, the voltages at different nodes in the circuit are recorded and analyzed.

A linear combination is performed on the voltages measured at different nodes using the coefficients B_1, B_2 and B_3 listed above. Firstly, a linear combination is performed on the diode voltages measured using the set up shown in Figure 14.

The output obtained after linear recombination of V_1, V_2 and V_3 recorded a TC of 0.5677ppm/°C, which is presented in comparison with the measured Vout as in Figure 41.

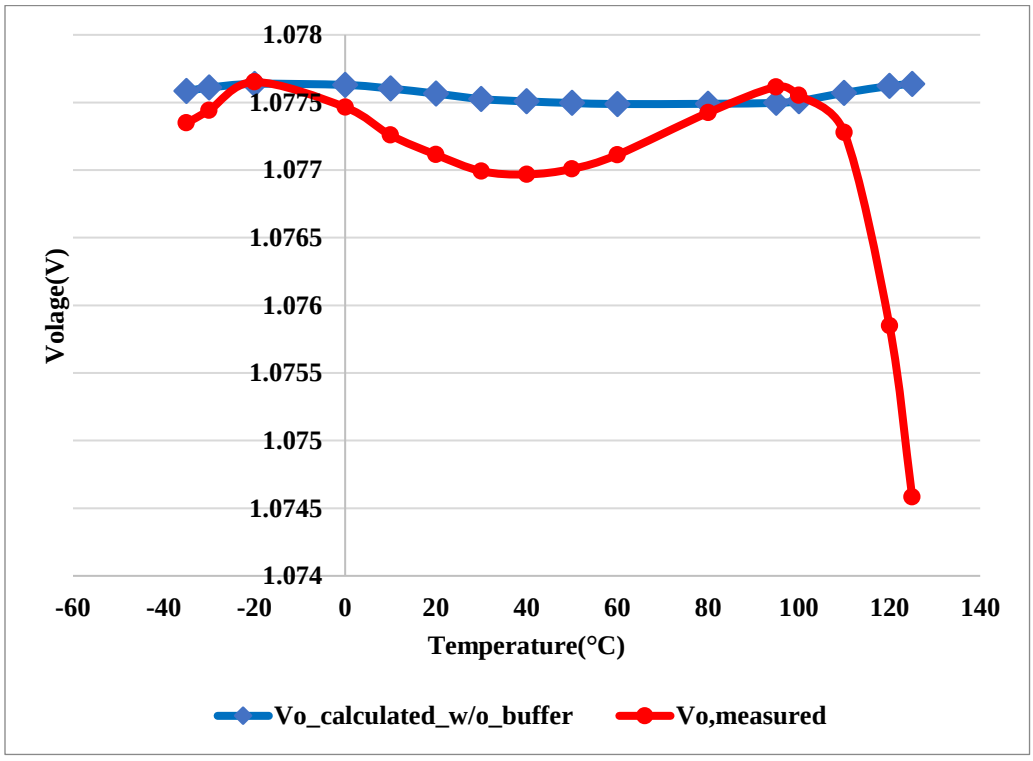


Figure 41:Measured and calculated V_{OUT} using V_{BE} measured without buffer

Next, a linear combination is performed on the diode voltages (V1, V2 and V3) measured in the presence of the buffers and the active circuitry (as in Figure 30) using B_1, B_2 and B_3. The linear recombination resulted in a voltage output having a TC of 12ppm/°C. A tail is observed at higher temperatures, similar to the measured V_{OUT} as shown in Figure 42. Figure 41 and 42 indicates a difference in the linearly recombined output using the diode voltages with and without the buffer. Results suggest that there is a difference in the diode voltage, measured with and without the buffer.

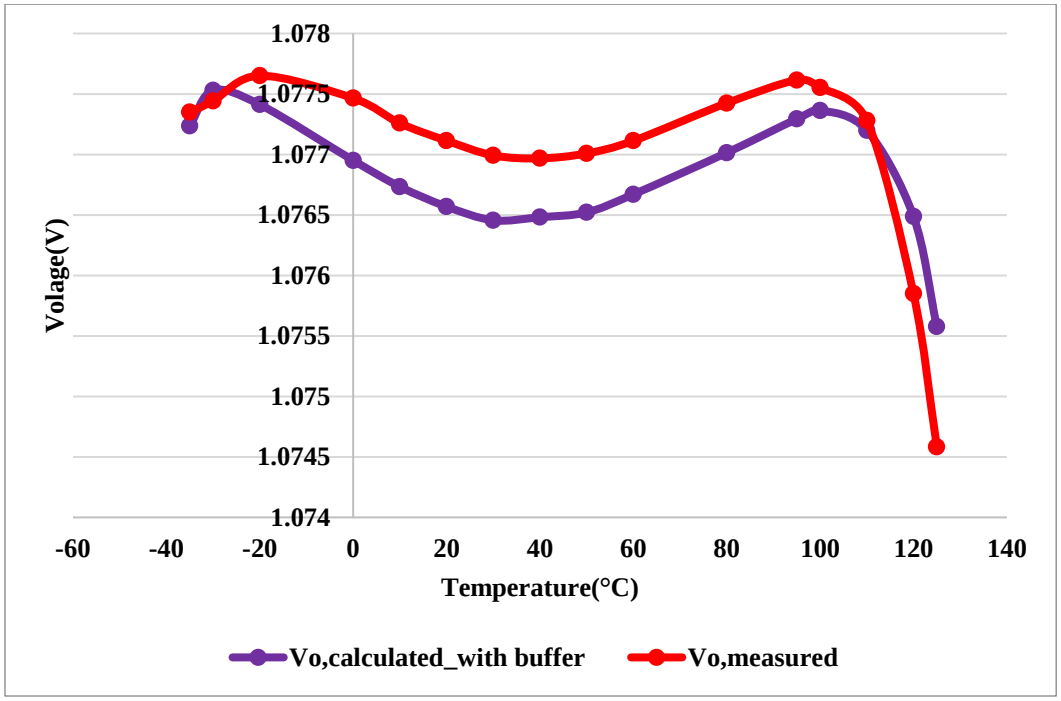


Figure 42: Measured and calculated V_{OUT} using V_{BE} measured with buffer

The voltages measured at the output of the buffers, V11, V22 and V33 were used for linear recombination and a similar tail is observed as shown in Figure 43. The output recorded a temperature coefficient of 19ppm/°C.

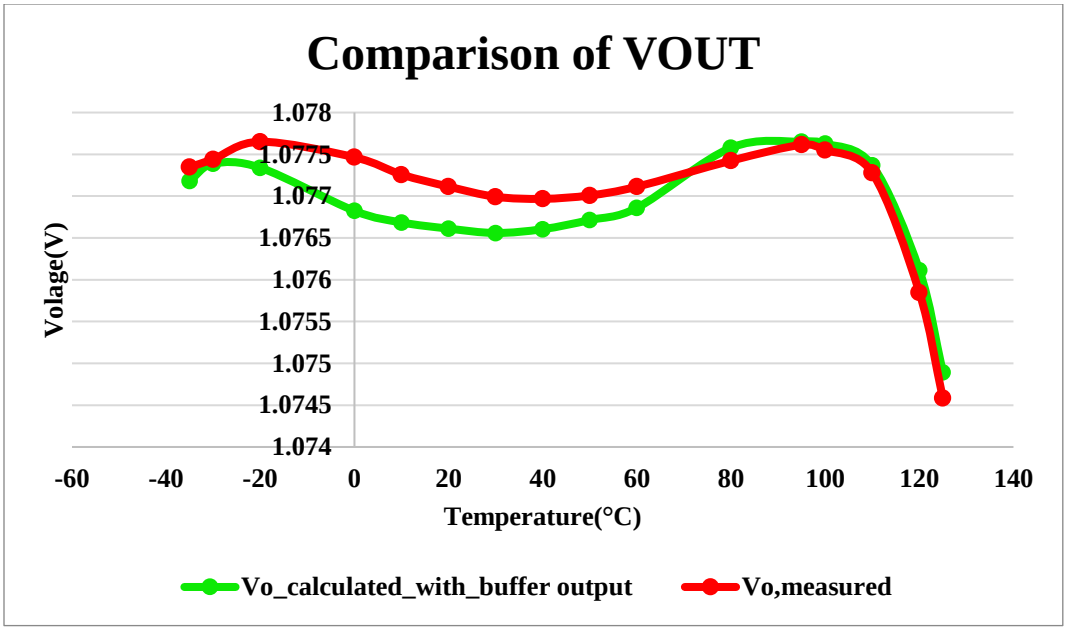


Figure 43: Measured and calculated V_{OUT} using V_{BE} measured with buffer output

Since it has been observed from Figure 41 and Figure 42 that there is a difference between the measured diode voltages with and without the buffer, it is investigated further. Figure 44 depicts the difference between the V_1, V_2 and V_3 measured with and without the buffer.

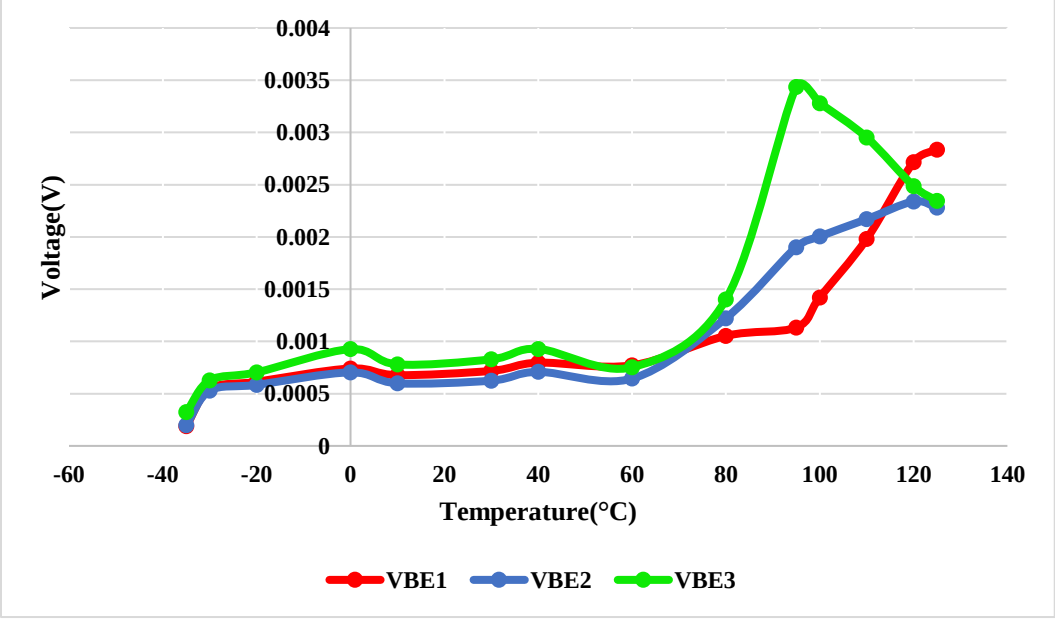


Figure 44: Difference between diode voltages with and without the buffers

It can be observed that the difference between the diode voltages increases with temperature. The difference lies within 1.5mV at temperatures ranging from -35°C to 85°C and increases at higher temperatures. This difference indicates a loading effect due to the presence of the buffer. Following the I-V characteristics of the diode, a change is voltage is induced by a change in current and the only source of current at the emitter node of the diode-connected BJT is the bias/offset current of the op amp used as a buffer as shown in Figure 30.

There are two significant sources of error being introduced by the op amp – Offset voltage and offset current. It was anticipated that the offset voltage of the op amp would be of a greater concern and a chopper amplifier, ADA4528, having a low offset voltage specification was chosen for the purpose.

From the datasheet specification, the maximum offset voltage across the temperature range of -40°C to 125°C is 4uV. The relative change in the output of the buffer caused by the offset voltage can be approximated as

Relative Change due to $V_{OS} = \frac{4uV}{700mV} * 100 \approx 5e\text{-}6\ \%$

The maximum offset current across the temperature range -40°C to 125°C is 1nA. The relative change in the diode current because of offset current can be estimated as

Relative change due to $I_{OS} = \frac{1nA}{10uA} * 100 \approx 0.01\%$.

Results imply that the offset current of the op amp has a significant error contribution among the external error sources.

The op-amp used as a buffer is found to have a significant loading effect and hence is not suitable for the implementation of the V_{GO} extraction concept at higher temperatures. The performance of the V_{GO} extraction circuit is calculated in the industrial temperature range, -

35°C to 85°C. ADA4258-2 was chosen due to the ultra-low offset voltage. But the error analysis indicates that the use of op-amps with lower bias currents can be used to implement the proposed V_{GO} extraction concept over the desired temperature range of -40°C to 125°C.

The measured temperature coefficient of V_{REF} is 4.57ppm/°C over the temperature range of -35°C to 85°C as shown in Figure 45.

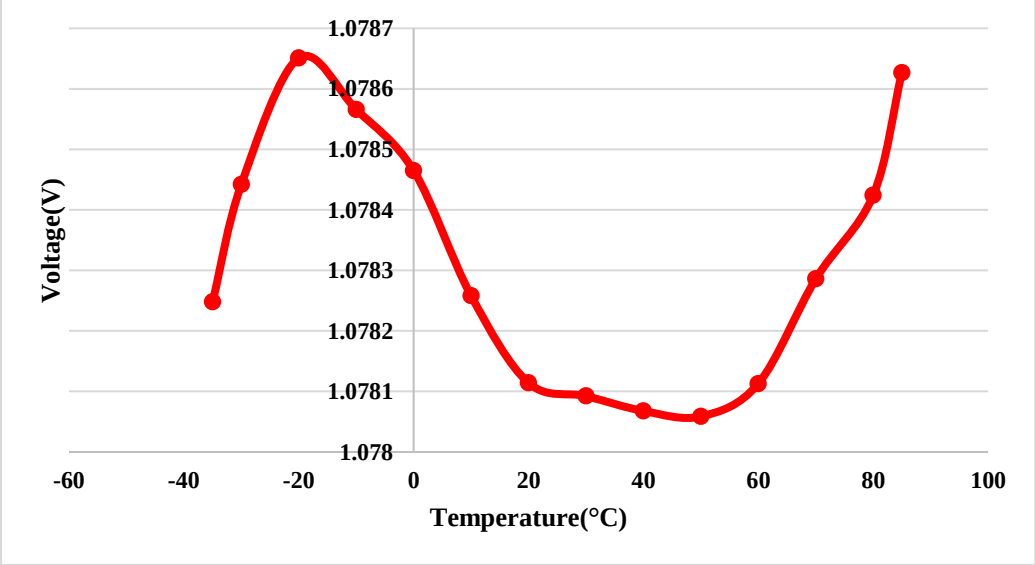


Figure 45:Measured V_{OUT} in the industrial temperature range

Another chip was tested similarly. The coefficients were determined as

B_1 = -7.7059

B_2 = 12.8569

B_3= -4.1513

The measured temperature coefficient of V_{REF} is 3.4ppm/°C over the industrial temperature range as shown in Figure 46.

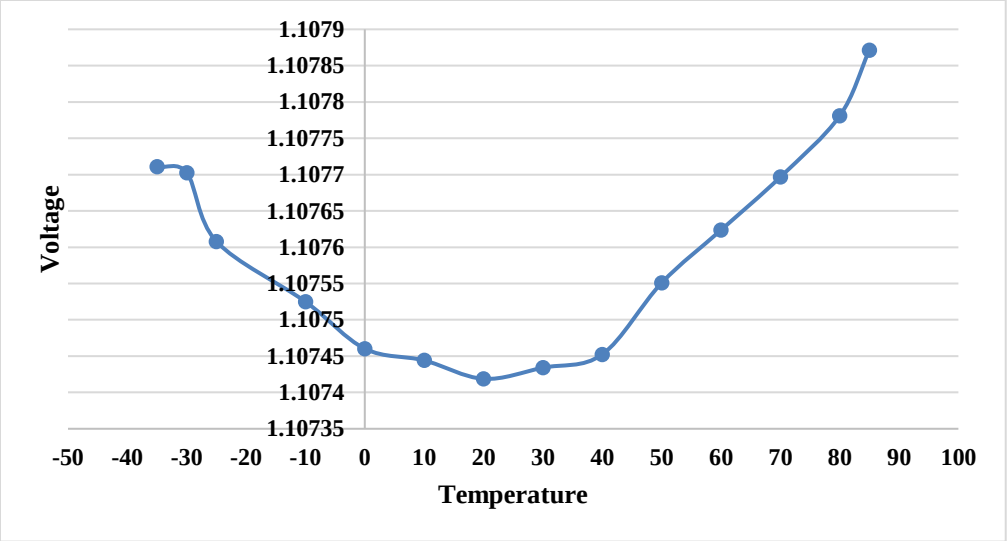


Figure 46: Measured V_{OUT}-Chip 2

A comparison of the performance of the proposed voltage reference generator with the state-of-the-art high precision voltage reference generators is presented in the Table.

Ref.	[24]	[25]	[16]	[26]	[27]	[28]	[29]	[30]	Proposed
Year	2012	2015	2011	2015	2014	2012	2015	2011	
Publication	JSSC	TCAS	JSSC	TED	TCAS	TCAS	ISSCC	TVLSI	
Reference (V)	0.6177	0.730	1.8	1.1402	0.767	1.285	1.21	0.4876	1.07
Temp range (°C)	-15-150°C	-40-120°C	-40-120°C	-55-125°C	-40-120°C	-40-100°C	-40-120°C	-40-110°C	-35-85°C
Best TC (ppm/°C)	**3.9**	**4.2**	**5**	**4.1**	**3.5**	**5**	**7**	**8.9**	**3.4**
Samples	5	8	61	8	8	5	-	5	2
Average TC (ppm/°C)	15.6	9.3	-	-	-	-	-	11.8	3.9

CHAPTER 7: SUMMARY AND FUTURE WORK

In this thesis, a bandgap voltage reference generator targeted at extracting the bandgap voltage of Silicon at 0K, was proposed, implemented and tested. The analytical expressions associated with the extraction concept were re-derived. Using analytical analysis, it is determined that a linear recombination of V_{BE}, V_{NL} and V_{PTAT} using suitable coefficients can isolate V_{GO} and the target was to determine the suitable coefficients for the process. A practical four-point fitting approach was proposed, with the simulation results achieving a TC of 0.17ppm/°C in the desired temperature of -40°C to 125°C. An analog domain implementation using buffers and a summing circuit was used to implement the idea.

The proposed concept was tested and validated using PCB measurements and various constraints were carefully studied. Two units were tested, and the measured temperature coefficient of the output voltage reference obtained are 3.4ppm/°C and 4.57ppm/°C across the industrial temperature range. The buffer circuit presented a loading effect, which deteriorated the performance of the bandgap circuit at higher temperatures. Since the offset current of the op amp is determined to be a dominant source of error in the system, future versions of the circuit need to be implemented using buffers that contribute to lower loading effect.

Most of the existing state-of-the-art curvature compensation circuits focus on the cancellation of the non-linearity in V_{BE}. Trimming at one or more temperatures is performed to achieve a temperature coefficient, even, in the single-ppm/°C range. In the chosen technique, the idea is to utilize discrete resistors, for implementing the coefficients. The technique is expected to compensate for all the neglected non-idealities, discussed in Chapter 3. The approach utilizes the base-emitter voltages across the diodes, which captures the effect

of all non-idealities and the coefficients are so chosen to take these effects into account. A comparison of the performance of the proposed circuit with the state-of-the-art circuits is presented in Chapter 6. Ma[27] reported a best temperature coefficient of 3.5ppm/°C over a 150°C temperature range. The proposed approach achieves a best TC of 3.4ppm/°C over a 120°C temperature range.

The loading effect of the buffer was determined to be the major error source in the circuit and a significant improvement in the performance should be attainable by suitable modifications. The future versions of the circuit need to be implemented using buffers that contribute to lower loading effect. Precision amps that has bias currents, which are in the order of femto-amperes can combat the issue and help achieve a better performance.

An on-chip implementation of the circuit will consume a significant amount of area since it requires a PTAT generator circuit, a ZTC current source, op amps utilized as buffers and an op-amp to implement the necessary equation and may not be optimal. Hence, attempts to integrate the circuits to minimize the area consumption needs to be investigated. Since the described technique is more of a preliminary approach to extract V_{GO}, it may be more efficient to come up with bootstrap techniques that will compensate for all the non-idealities.

It would also be interesting to investigate the effect of non-idealities described in Chapter 3 on this approach. Since, the layout of the key diodes affects the non-idealities, modifying certain aspects of the layout such as number of contacts, base-width, distance between emitter and collector, etc., may be investigated and the variation in the base-emitter voltages and the coefficients may be analyzed and an optimal layout for the required application may be chosen.

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APPENDIX. TEMPERATURE DEPENDENCE OF V_{BE}

A simplified derivation associated with the Tsividis equation [14] is presented here. The collector current of a BJT can be expressed as

$$I_C = I_S e^{\frac{qV_{BE}}{V_T}},$$

$$V_{BE} = \left(\frac{kT}{q}\right) \ln\left(\frac{I_C}{I_s}\right)$$

$$I_s(T) = \frac{kTAn_i^2(T)\mu_P(T)}{G_B(T)}$$

where k is the Boltzmann constant A is the area of the base-emitter junction, n_i is the intrinsic carrier concentration, μ_P is the effective minority carrier diffusion constant in the base, G_B is the Gummel number.

$$n_i^2(T) \propto T^3 e^{\frac{-qV_G(T)}{kT}}$$

$\mu_P(T) \propto T^{-m}$, where m is a process parameter

$$I_S = CT^{4-m} e^{-\left(\frac{qV_G(T)}{kT}\right)}$$

$I_S = CT^{\eta} e^{-\left(\frac{qV_G(T)}{kT}\right)}$, where η = 4-m

$$I_c(T) = I_s(T) e^{\frac{q(V_{BE}(T) - V_G(T))}{kT}}$$

$$I_c(T_r) = I_s(T_r) e^{\frac{q(V_{BE}(T_r) - V_G(T_r))}{kT_r}}$$

$$\frac{I_c(T)}{I_c(T_r)} = \left(\frac{T}{T_r}\right)^{\eta} e^{\frac{q}{k}\left(\frac{V_{BE}(T)}{T} - \frac{V_{BE}(T_r)}{T_r} - \left(\frac{V_G(T)}{T} - \frac{V_G(T_r)}{T_r}\right)\right)}$$

Bandgap voltage, $V_G(T)$ is assumed to have a linear temperature dependence,

$$V_G(T) = V_{GOr} + \varepsilon_r T$$

$$V_G(T_r) = V_{GOr} + \varepsilon_r T_r$$

$$\ln\left(\frac{I_c(T)}{I_c(T_r)}\right) = \eta \ln\left(\frac{T}{T_r}\right) + \frac{q}{kT}(V_{BE}(T) - V_{GOr}) - \frac{q}{kT_r}(V_{BE}(T_r) - V_{GOr})$$

If collector current is proportional to some power (δ) of temperature, the above expression can be modified and rearranged as shown below.

$I_c(T)\ \alpha\ T^{\delta}$

$I_c(T_r)\ \alpha\ T_r^{\delta}$

$$V_{BE}(T) = V_{GOr} + T\left(\left(\frac{(V_{BE}(T_r) - V_{GOr})}{T_r}\right) - (\eta - \delta)\frac{k}{q}\ln(T_r)\right) + T\ln(T)\left(\left(\frac{-k}{q}\right)(\eta - \delta)\right)$$